DSND8GXXX3M

3.3V/1.8V, x8/x16 8G-BIT NAND FLASH

Documents title

8Gbit (1Gx8Bit, 512Mx16Bit) NAND FLASH

Revision History

Revision No.	History	Date	Remark
0.0	Initial Draft	May 30, 2019	preliminary
0.1	Modify 1.8V VCC range	Jul 8, 2019	
0.2	Modify 5th byte of ID table	Jul 9, 2019	
0.3	Add 105°C T_A support	Mar 20, 2020	
0.4	Modify serial access time parameters	Apr 7, 2020	
0.5	Update tREA time	Jul 10, 2020	
0.6	Optimize package drawings	Jun 28, 2026	
0.7	Align t_{RC}&t_{WC} of 105°C to 85°C	Sep 16, 2026	

Datasheet can be modified without any notice!

FEATURES

■ x8/x16 I/O BUS

- NAND Interface
- ADDRESS / DATA Multiplexing

■ SUPPLY VOLTAGE

- VCC = 1.8/2.7/3.3 Volt core supply voltage for Program, Erase and Read operations

■ PAGE READ / PROGRAM

- x8 : (2048+64 spare) byte
- x16: (1024+32 spare) word page
- Synchronous Page Read Operation
- Random access : 25us (Max)
- Serial access : 30ns (1.8V)
  20ns (2.7/3.3V)
- Page program time : 200us (Typ)

■ PAGE COPY BACK

- Fast data copy without external buffering

■ CACHE PROGRAM

- Internal buffer to improve the program throughput

■ READ CACHE

■ LEGACY/ONFI 1.0 COMMAND SET

■ FAST BLOCK ERASE

- Block size :
  x8 : (128K + 4K) bytes
  x16: (64K+2K) words
- Block erase time : 2ms (Typ)

■ MEMORY CELL ARRAY

- x8 : (2K + 64) bytes x 64 pages x 4096 blocks x 2die
- x16: (1K + 32) words x 64 pages x 4096 blocks x 2die

■ ELECTRONIC SIGNATURE

- Manufacturer Code
- Device Code

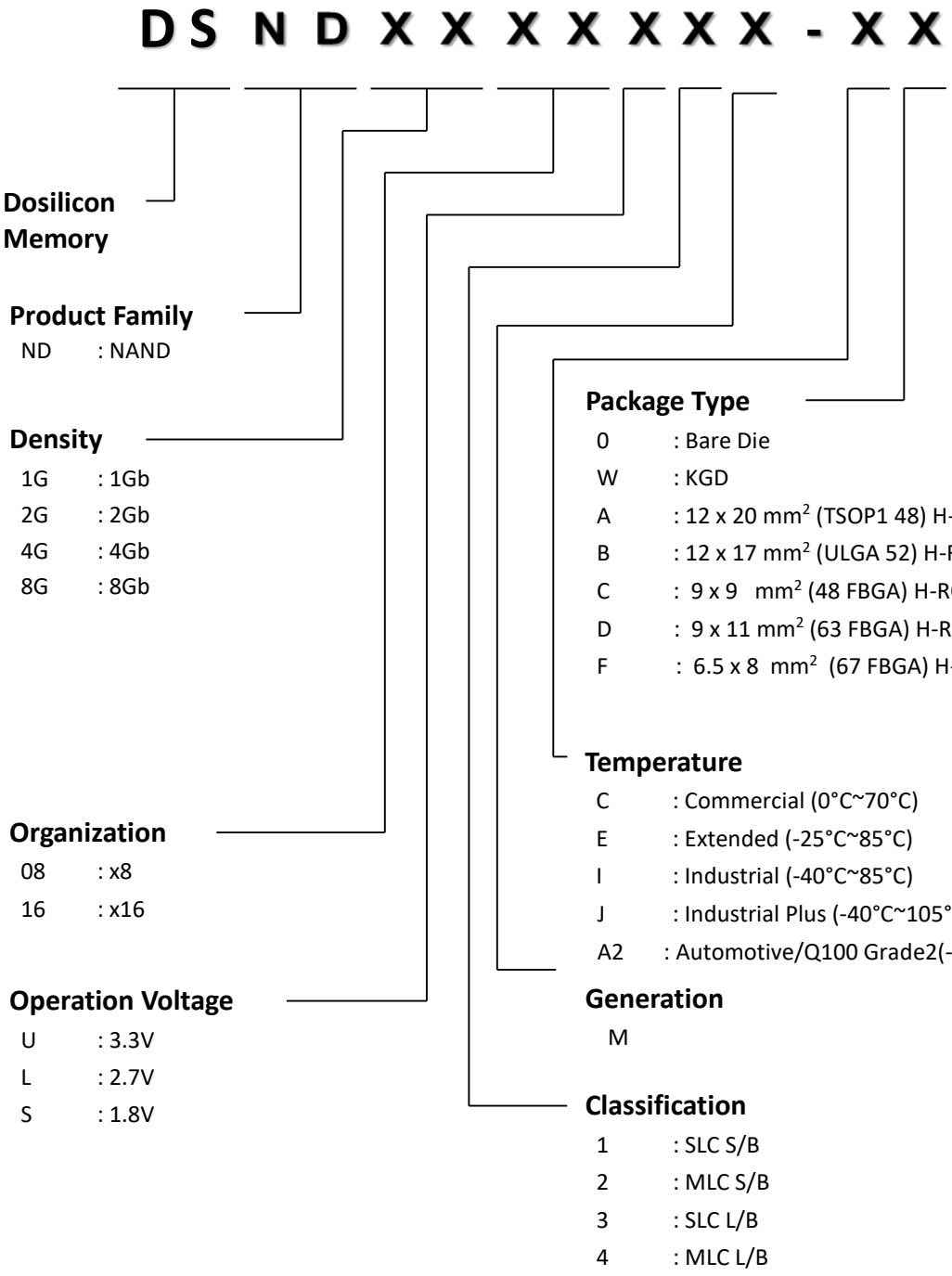
■ STATUS REGISTER

■ HARDWARE DATA PROTECTION

■ DATA RETENTION

- 100K Program / Erase cycles
- Data retention : 10 Years(4bit/512byte ECC)

Part Numbering System



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1 SUMMARY DESCRIPTION

DSND8GXXX3M is a **1Gx8bit** with spare **32Mx8 (x8), 512Mx16bit** with spare **16Mx16(x16)** bit capacity.
The device is offered in 3.3/1.8 Vcc Power Supply, and with x8 and x16 I/O interface.
The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains **8192 blocks**, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells.
Memory array is split into 2 die and 2 planes/die, each of plane consisting of **2048** blocks.
Program operation allows the 2112-byte page writing in typical 200us and an erase operation can be performed in typical **2 ms** on a 128K-byte block.
In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane).
Data in the page can be read out at **20ns** cycle time per word **(3.3V version)**, and at **30ns** cycle time per word **(1.8V version)**.
The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint.
Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP# input pin.
This device supports ONFI 1.0 specification.
The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal.

The **DSND8GXXX3M** is available in the following packages : 48 - TSOP1 12x20 mm package, FBGA63 9x11 mm.

1.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE
DSND8G08S3M	X8	1.7 – 1.95 Volt	VFBGA, TSOP
DSND8G08U3M	X8	2.7 – 3.6 Volt	VFBGA, TSOP

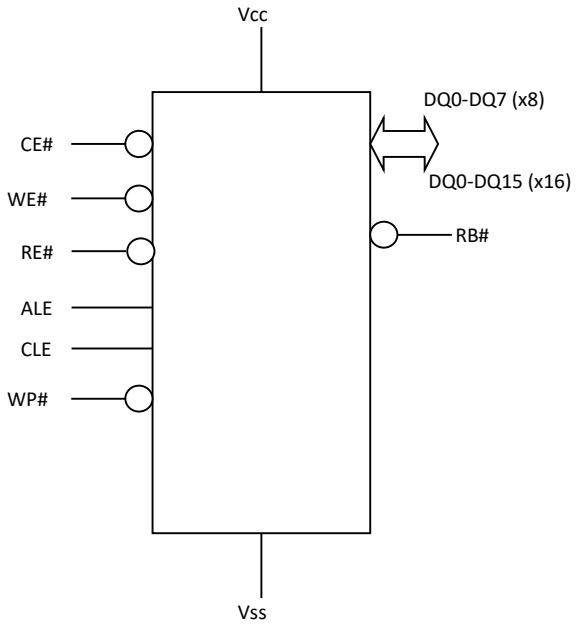


Figure 1: Logic Diagram

DQ7 - DQ0	Data Input / Outputs (x8/x16)
DQ15 – DQ8	Data Input / Outputs (x16)
CLE	Command latch enable
ALE	Address latch enable
CE#	Chip Enable
RE#	Read Enable
WE#	Write Enable
WP#	Write Protect
RB#	Ready / Busy
Vcc	Power supply
Vss	Ground
NC	No Connection

Table 1: signal names

1.2 Pin description

Pin Name	Description
DQ0-DQ7(x8) **DQ0-DQ15(x16)**	DATA INPUTS/OUTPUTS The DQ pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable (WE#). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	COMMAND LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	ADDRESS LATCH ENABLE This input activates the latching of the DQ inputs inside the Command Register on the Rising edge of Write Enable (WE#).
CE#	CHIP ENABLE This input controls the selection of the device. When the device is busy CE# low does not deselect the memory.
WE#	WRITE ENABLE This input acts as clock to latch Command, Address and Data. The DQ inputs are latched on the rise edge of WE#.
RE#	READ ENABLE The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WP#	WRITE PROTECT The WP# pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
RB#	READY BUSY The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	SUPPLY VOLTAGE The VCC supplies the power for all the operations (Read, Write, Erase). An internal lock circuit prevent the insertion of Commands when V_{CC} is less than V_{LKO}
V_{SS}	GROUND
NC / DNU	NOT CONNECTED / DON'T USE

Table 2 : pin description

Notes:
1. A 0.1 µF capacitor should be connected between the VCC Supply Voltage pin and the VSS Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3 Functional block diagram

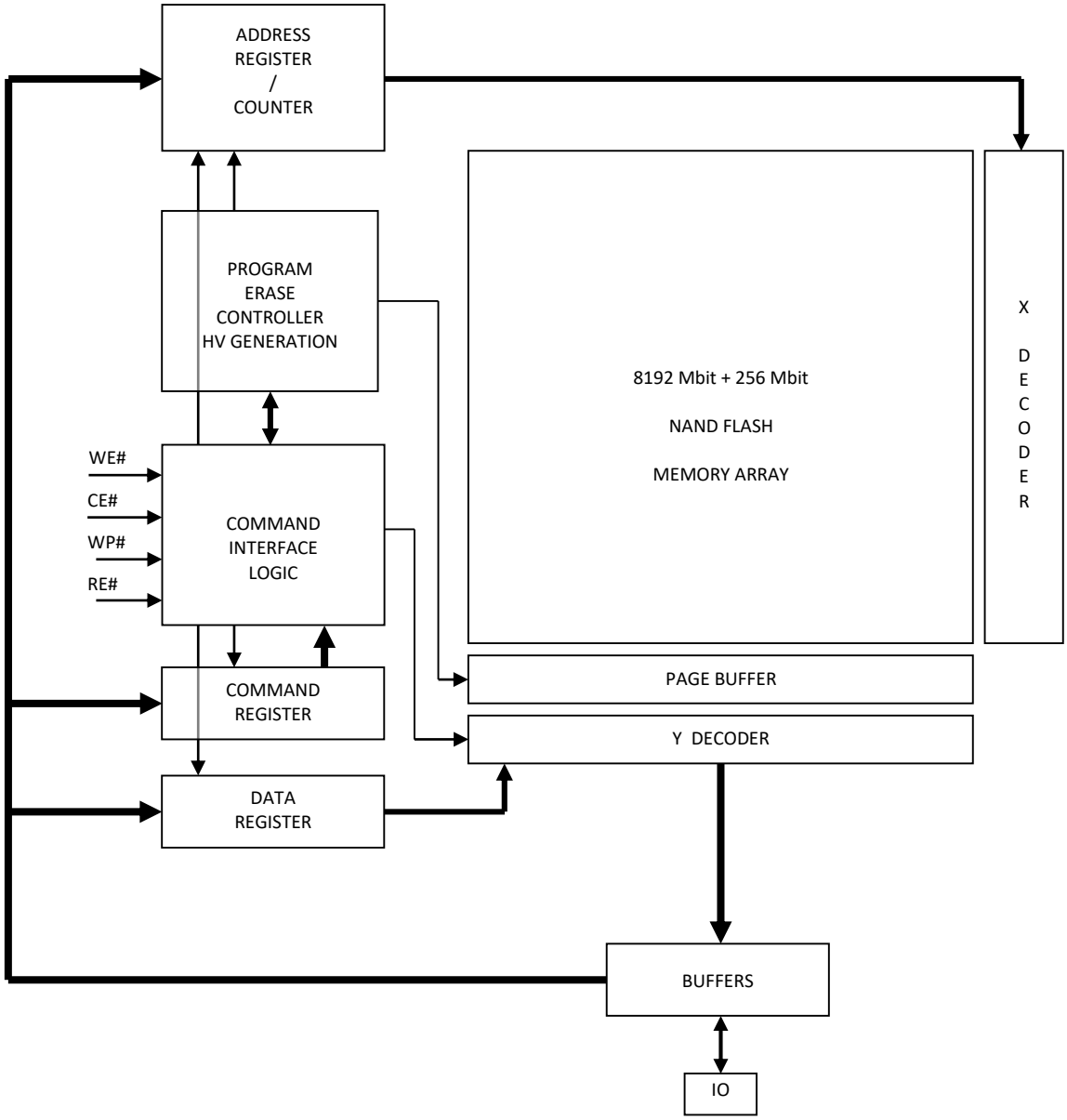


Figure 2 : block description

1.4 Address role

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	0	0	0	0
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle (*)	A28	A29	A30	0	0	0	0	0

Table 3 : Address Cycle Map (x8)

A0 – A11 : byte (column) address in the page
A12 – A17 : page address in the block
A18 : plane address (for multi-plane operations) / block address (for normal operations)
A19 – A30 : block address (A30 is die select)

	DQ0	DQ1	DQ2	DQ3	DQ4	DQ5	DQ6	DQ7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	0	0	0	0	0
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26
5th Cycle (*)	A27	A28	A29	0	0	0	0	0

Table 4 : Address cycle Map (x16)

A0 – A10 : word (column) address in the page
A11 – A16 : page address in the block
A17 : plane address (for multi-plane operations) / block address (for normal operations)
A18 – A29 : block address (A29 is die select)

1.5 Command Set

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
READ	00h	30h	-	-	
READ FOR COPY-BACK	00h	35h	-	-	
READ ID	90h	-	-	-	
RESET	FFh	-	-	-	Yes
PAGE PGM (start) / CACHE PGM (end)	80h	10h	-	-	
CACHE PGM (Start/continue)	80h	15h	-	-	
COPY BACK PGM	85h	10h	-	-	
LEGACY MULTI PLANE PROGRAM	80h	11h	81h	10h	
ONFI MULTIPLANE PROGRAM	80h	11h	80h	10h	
LEGACY MULTIPLANE CACHE PGM (start/cont)	80h	11h	81h	15h	
ONFI MULTIPLANE CACHE PGM (start/cont)	80h	11h	80h	15h	
LEGACY MULTIPLANE CACHE PGM (end)	80h	11h	81h	10h	
ONFI MULTIPLANE CACHE PGM (end)	80h	11h	80h	10h	
LEGACY MULTI PLANE COPY BACK PROGRAM	85h	11h	81h	10h	
ONFI MULTIPLANE COPYBACK PGM	85h	11h	85h	10h	
BLOCK ERASE	60h	D0h	-	-	
LEGACY MULTI PLANE BLOCK ERASE	60h	60h	D0h	-	
ONFI MULTIPLANE BLOCK ERASE	60h	D1h	60h	D0h	
READ STATUS REGISTER	70h	-	-	-	Yes
READ STATUS ENHANCED	78h				Yes
RANDOM DATA INPUT	85h	-	-	-	
RANDOM DATA OUTPUT	05h	E0h	-	-	
READ CACHE (SEQUENTIAL)	31h				
READ CACHE ENHANCED (RANDOM)	00h	31h	-	-	
READ CACHE END	3Fh	-	-	-	
READ PARAMETER PAGE	ECh				

Table 5 : Command Set

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Data Output (on going)	
X	X	L(1)	H	H	X	Data Output (suspended) (2)	
L	L	L	H	H	X	Busy time in Read	
X	X	X	X	X	H	Busy time in Program	
X	X	X	X	X	H	Busy time in Erase	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V / V_{CC}	Stand By	

Table 6 : Mode Selection

2 BUS OPERATION

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 3 and Table 20 for details of the timings requirements. Command codes are always applied on IO<7:0>, disregarding the bus configuration (X8/X16).

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high. See Figure 4 and Table 20 for details of the timings requirements. Addresses are always applied on IO<7:0>, disregarding the bus configuration (X8/X16).

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 5 and Table 20 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the lock status and the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 6,7,8 and Table 20 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation do not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

2.6 Standby.

In Standby the device is deselected, outputs are disabled and Power Consumption reduced.

3 DEVICE OPERATION

3.1 Page Read.

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing **00h** and **30h** to the command register along with **5** address cycles. In two consecutive read operations, the second one does need 00h command, which four address cycles and **30h** command initiates that operation. Second read operation always requires setup command if first read operation was executed using also random data out command.
Two types of operations are available: random read , serial page read. The random read mode is enabled when the page address is changed. The **2112** bytes (X8 device) or **1056** words (X16 device) of data within the selected page are transferred to the data registers in less than **25us(tR).** The system controller may detect the completion of this data transfer (tR) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in **20ns cycle time (3.3V version) or 30ns cycle time (1.8V version)** by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.
The device may output random data in a page instead of the consecutive sequential data by writing random data output command.
The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.
Any operation other than read or random data output causes device to exit read mode.
Check Figure 10,11,12 as references.

3.2 Read Cache

The Read Cache function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command, as defined in **3.1**, shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence.
The Read Cache function may be issued after the Read function is complete (SR[6] is set to one). The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00h. If the host does not enter an address to retrieve, the next sequential page is read. When the Read Cache function is issued, SR[6] is cleared to zero (busy). After the operation is begun SR[6] is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3Fh command. The host may begin to read data from the page register when SR[6] is set to one (ready). When the 31h and 3Fh commands are issued, SR[6] shall be cleared to zero (busy) until the page has finished being copied from the Flash array. The host shall not issue a sequential Read Cache (31h) command after the last page of the device is read.
Figure 13 defines the Read Cache behavior and timings for the beginning of the cache operations subsequent to a Read command being issued. SR[6] conveys whether the next selected page can be read from the page register. Figure 14 defines the Read Cache behavior and timings for the end of cache operation.

3.3 Page Program.

The device is programmed basically by page, but it does allow multiple partial page programming of a word or consecutive bytes up to 2112 (X8 device) or words up to 1056 (X16 device), in a single page program cycle.
A page program cycle consists of a serial data loading period in which up to **2112 bytes** (X8 device) or **1056 words** (X16 device) of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command **(80h)**, followed by **5** cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (**85h**). Random data input may be operated multiple times regardless of how many times it is done in a page.

The Page Program confirm command **(10h)** initiates the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register. Figure 15,16 detail the sequence.

3.4 Multiple plane program

Device supports multiple plane program: it is possible to program 2 pages in parallel, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins with inputting the Serial Data Input command (80h), followed by the **5** cycle address inputs and serial data for the 1st page. Address for this page must be in the 1st plane (A<18>=0). The device supports random data input exactly same as in the case of page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and devices becomes busy for a short time (t_{DBSY}). Once it has become ready again, either the "81h" or "80h" command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be in the 2nd plane (A<18>=1). Program Confirm command (10h) makes parallel programming of both pages to start. Figure 17 details this sequences.
User can check operation status by monitoring RB# pin or reading status register commands (70h or 78h), as if it were a normal page program; read status register command is also available during Dummy Busy time (t_{DBSY}).
In case of fail in any of 1st and 2nd page program, fail bit of status register will be set; however, in order to know which page failed, ONFI 1.0 "read status enhanced" command must be issued Refer to section **3.12** for further info.

3.5 Copy-Back Program.

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "**35h**" command and the address of the source page moves the whole 2112byte (X8 device) or 1056word (X16 device) data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (**85h**) with the address cycles of destination page may be written. The Program Confirm command (**10h**) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 18.

3.6 Multiple plane copy back Program

As for page program, device supports Multi-plane copy back program with exactly same sequence and limitations. Multi plane copy back program must be preceded by 2 single page read for copy back command sequences (1st page must be read from the 1st plane and 2nd page from the 2nd plane).
Multi-plane copy back cannot cross plane boundaries : the contents of the source page of one device plane can be copied only to a destination page of the same plane .
It is represented in Figure 19.

3.7 Cache Program

Cache Program is an extension of the standard page program which is executed with two 2112 bytes(x8 device) or 1056 words(x16 device) registers, the data and the cache register.

In short, the cache program allows data insertion for one page while program of another page is under execution. Cache program is available only within a block.
After the serial data input command (80h) is loaded to the command register, followed by **5** cycles of address, a full or partial page of data is latched into the cache register.
Once the cache write command (15h) is loaded to the command register, the data in the cache register is transferred into the data register for cell programming. At this time the device remains in Busy state for a short time (t_{PCBSY}). After all data of the cache register are transferred into the data register, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence (80h-15h).
The busy time following the first sequence 80h – 15h equals the time needed to transfer the data of cache register to the data register. Cell programming of the data of data register and loading of the next data into the cache register is consequently processed through a pipeline model.
In case of any subsequent sequence 80h – 15h, transfer from the cache register to the data register is held off until cell programming of current data register contents is complete; till this moment the device will stay in a busy state (t_{PCBSY}).
Read Status commands (70h) may be issued to check the status of the different registers, and the pass/fail status of the cached program operations. It is represented in Figure 20.
More in detail:
a) the Cache-Busy status bit I/O<6> indicates when the cache register is ready to accept new data.
b) the status bit I/O<5> can be used to determine when the cell programming of the current data register contents is complete
c) the cache program error bit I/O<1> can be used to identify if the previous page (page N-1) has been successfully programmed or not in cache program operation. The latter can be polled upon I/O<6> status bit changing to "1" .
d) the error bit I/O<0> is used to identify if any error has been detected by the program / erase controller while programming page N. The latter can be polled upon I/O<5> status bit changing to "1".
I/O<1> may be read together with I/O<0> .
If the system monitors the progress of the operation only with R/B#, the last page of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

3.8 Multi-plane Cache Program

The device supports multi-plane cache program, which enables high program throughput by programming two pages in parallel while exploiting the data and cache registers of both planes to implement cache.
The device supports both the Legacy and ONFI 1.0 command sets.

The command sequence can be summarized as follows :
a) Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<18>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation.
b) The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY).
c) Once device returns to ready again, 81h (or 80h) command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<18>=1). The data of 2nd page other than those to be programmed do not need to be loaded.
d) Cache Program confirm command (15h) Once the cache write command (15h) is loaded to the command register, the data in the cache registers is transferred into the data registers for cell programming. At this time the device remains in Busy state for a short time (t_{PCBSY}). After all data of the cache registers are transferred into the data registers, the device returns to the Ready state, and allows loading the next data into the cache register through another cache program command sequence.
The sequence 80h-...- 11h...-...81h...-...15h (or the corresponding ONFI 80h-...- 11h...-...80h...-...15h) can be iterated, and any new time the device will be busy for a for the t_{PCBSY} time needed to complete cell programming of current data registers contents, and transfer from cache registers can be allowed.
The sequence to end multi-plane cache program is 80h-...- 11h...-...81h...-...10h (or 80h-...- 11h...-...80h...-...10h for the ONFI 1.0 case) .
Figure 21 shows the command sequence for the multi plane cache program operation for the two protocols.
Multi-plane Cache program is available only within two paired blocks belonging to the two planes..

User can check operation status by R/B# pin or read status register commands (70h or 78h)
If user opts for 70h, Status register read will provide a “global” information about the operation in the two planes . More in detail:
a) I/O<6> indicates when both cache registers are ready to accept new data.
b) I/O<5> indicates when the cell programming of the current data registers is complete
c) I/O<1> identifies if the previous pages in both planes (pages N-1) have been successfully programmed or not. The latter can be polled upon I/O<6> status bit changing to "1" .
d) I/O<0> identifies if any error has been detected by the program / erase controller while programming the two pages N. The latter can be polled upon I/O<5> status bit changing to "1".
See Table 7 for more details

If the system monitors the progress of the operation only with R/B#, the last pages of the target program sequence must be programmed with Page Program Confirm command (10h). If the Cache Program command (15h) is used instead, the status bit I/O<5> must be polled to find out if the last programming is finished before starting any other operation.

3.9 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in **3** cycles initiated by an Erase Setup command **(60h).** The Erase Confirm command (**D0h**) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.
At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 22 **Figure** details the sequence.

3.10 Multiple plane Erase

Multiple plane erase, allows parallel erase of two blocks in parallel, one per each memory plane.
Two different command sequences are allowed in these case, Legacy and ONFI 1.0.
In case of Legacy, Block erase setup command (60h) must be repeated two times, followed by 1st and 2nd block address respectively (**3** cycles each). As for block erase, D0h command makes embedded operation to start. In this case, multiplane erase does not need any Dummy Busy Time between 1st and 2nd block insertion.
See Figure 23 for details.
As an alternative, the ONFI 1.0 multiplane command protocol can be used , with 60h erase setup followed by 1st block address and D1h first confirm, 60h erase setup followed by 2nd block address and D0h (multiplane confirm) . Between the two block-related sequences, a short busy time TIEBSY will occur. See Table 19 and Figure 24 for details.
Address limitation required for multiple plane program applies also to multiple plane erase. Also operation progress can be checked like in the multiple plane program through Read Status Register, or ONFI 1.0 Read Status Enhanced .

3.11 Read Status Register.

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing **70h** command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when RB# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to Table 7 for specific Status Register definitions, and Figure 8 for specific timings requirements. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (**00h**) should be given before starting read cycles.

3.12 Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases :

- on **a specific plane** in case of multi-plane operations in the same die.

Figure 9 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest.

Refer to Table 7 for specific Status Register definition. The command register remains in Status Read mode until further commands are issued.

3.13 Read Status Register field definition

Table 7 below lists the meaning of each bit of Read Status Register and Read Status Enhanced

IO	Page Program	Block Erase	Read	Cache Read	Cache Program/ Cache reprogram	CODING
0	Pass / Fail	Pass / Fail	NA	NA	Pass/Fail	N page Pass: '0' Fail: '1'
1	NA	NA	NA	NA	Pass/Fail	N-1page Pass: '0' Fail: '1'
2	NA	NA	NA	NA	NA	-
3	NA	NA	NA	NA	NA	-
4	NA	NA	NA	NA	NA	-
5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready /Busy	Active: '0' Idle:'1'
6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Data cache Read/Busy Busy: '0' Ready:'1'
7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected: '0' Not Protected: '1'

Table 7 : Status Register Coding

3.14 Read ID.

The device contains a product identification mode, initiated by writing **90h** to the command register, followed by an address input of 00h.

DENSITY	ORG.	VCC	1st	2nd	3rd	4th	5th
8Gbit	X8	3.3V	E5h	D3h	D1h	95h	5Ah
	X16	3.3V	E5h	C3h	D1h	D5h	5Ah
	X8	1.8V	E5h	A3h	D1h	15h	5Ah
	X16	1.8V	E5h	B3h	D1h	55h	5Ah

Table 8: Read ID for supported configurations

DEVICE IDENTIFIER BYTE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell type,….
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 9 : Read ID bytes meaning

	Description	DQ7	DQ6	DQ5-4	DQ3-2	DQ1-0
Internal Chip Number	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of simultaneously programmed pages	1 2 4 8			0 0 0 1 1 0 1 1		
Interleaved program between multiple dice	Not Supported Supported		0 1			
Cache Program	Not Supported Supported	0 1				

Table 10 : 3rd byte of Device Identifier Description

	Description	DQ7	DQ6	DQ5-4	DQ3	DQ2	DQ1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512 Byte)	8 16					0 1	
Block Size (Without Spare Area)	64KB 128KB 256KB 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				
Serial Access Time	30ns 20ns Reserved Reserved	0 1 0 1			0 0 1 1		

Table 11 : 4th Byte of Device Identifier Description

	Description	DQ7	DQ6-4	DQ3-2	DQ1-0
ECC Level	1bit/512Byte 2bit/512Byte 4bit/512Byte 8bit/512Byte				0 0 0 1 1 0 1 1
Plane Number	1 2 4 8			0 0 0 1 1 0 1 1	
Plane Size (Without Spare Area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1		
Reserved		0			

Table 12 : 5th Byte of Device Identifier Description

To retrieve the ONFI signature, the command 90h together with an address of 20h shall be entered (i.e. it is not valid to enter an address of 00h and read 36 bytes to get the ONFI signature). The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4Fh, 'N' = 4Eh, 'F' = 46h, and 'I' = 49h. Reading beyond four bytes yields indeterminate values. Figure 26 shows the operation sequence .

3.15 Reset.

The device offers a reset feature, executed by writing **FFh** to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. Refer to Table 7 for device status after

reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written (see Figure 27).

3.16 Read Parameter Page

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timings and other behavioral parameters. Figure 28 defines the Read Parameter Page behavior.
Values in the parameter page are static and shall not change. The host is not required to read the parameter page after power management events.
The Change Read Column command can be issued during execution of the Read Parameter Page to read specific portions of the parameter page.
Read Status may be used to check the status of Read Parameter Page during execution. After completion of the Read Status command, 00h shall be issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.
Read Status Enhanced shall not be used during execution of the Read Parameter Page command.

3.17 Parameter Page Data Structure Definition

Table 13 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.
Values are reported in the parameter page in units of bytes when referring to items related to the size of data access (as in an 8-bit data access device). For example, the chip will return how many data *bytes* are in a page. For a device that supports 16-bit data access, the host is required to convert byte values to word values for its use. Unused fields should be cleared to 0h.
For more detailed information about Parameter Page Data bits, refer to ONFI Specification 1.0 section 5.4.1

Byte	O/M	Description
		Revision information and features block
0-3	M	Parameter page signature Byte 0: 4Fh, "O" Byte 1: 4Eh, "N" Byte 2: 46h, "F" Byte 3: 49h, "I"
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copyback 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache 20ntegrit 0 1 = supports Page Cache Program command
10-31		Reserved (0)
		Manufacturer information block
32-43	M	Device manufacturer (12 ASCII characters)
44-63	M	Device model (20 ASCII characters)
64	M	JEDEC manufacturer ID
65-66	O	Date code
67-79		Reserved (0)

Byte	O/M	Description
	Memory organization block	
80-83	M	Number of data bytes per page
84-85	M	Number of spare bytes per page
86-89	M	Number of data bytes per partial page
90-91	M	Number of spare bytes per partial page
92-95	M	Number of pages per block
96-99	M	Number of blocks per logical unit (LUN)
100	M	Number of logical units (LUNs)
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles
102	M	Number of bits per cell
103-104	M	Bad blocks maximum per LUN
105-106	M	Block endurance
107	M	Guaranteed valid blocks at beginning of target
108-109	M	Block endurance for guaranteed valid blocks
110	M	Number of programs per page
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints
112	M	Number of bits ECC correctability
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support
115-127		Reserved (0)
	Electrical parameters block	
128	M	I/O pin capacitance
129-130	M	Timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1
131-132	O	Program cache timing mode support 6-15 Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0
133-134	M	t_{PROG} Maximum page program time (µs)
135-136	M	t_{BERS} Maximum block erase time (µs)
137-138	M	t_R Maximum page read time (µs)
139-163		Reserved (0)
	Vendor block	
164-165	M	Vendor specific Revision number
166-253		Vendor specific
254-255	M	Integrity CRC

	Redundant Parameter Pages

Byte	O/M	Description
256-511	M	Value of bytes 0-255
512-767	M	Value of bytes 0-255
768+	O	Additional redundant parameter pages

Table 13 : Parameter page data

Note : “O” stands for Optional, “M” for Mandatory

4 Device Parameters

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number, 8Gb	N_{VB}	8032	-	8192	Blocks

Table 14: Valid Blocks Number

Symbol	Parameter	Value			Unit
		1.8V	2.7V	3.3V	
T_A	Ambient Operating Temperature	0 to 70	0 to 70	0 to 70	°C
	Ambient Operating Temperature	–40 to 85	–40 to 85	–40 to 85	°C
	Ambient Operating Temperature	–40 to 105	–40 to 105	–40 to 105	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	–50 to 125	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	–65 to 150	–65 to 150	°C
V_{IO}	Input or Output Voltage	–0.6 to 2.7	–0.6 to 4.6	–0.6 to 4.6	V
V_{CC}	Supply Voltage	–0.6 to 2.7	–0.6 to 4.6	–0.6 to 4.6	V

Table 15: Absolute maximum ratings

.

Parameter		Symbol	Test Conditions	1.8Volt			2.7Volt			3.3Volt			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC} = 50ns, CE#=V_{IL}, I_{OUT}=0mA	-	10	20	-	15	30	-	15	30	mA
	Program	I_{CC2}	-	-	10	20	-	15	30	-	15	30	mA
	Erase	I_{CC3}	-	-	10	20	-	15	30	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	CE#=V_{IH}, WP#=0V/V_{CC}	-	-	1	-		1			1	mA
Stand-By Current (CMOS)		I_{CC5}	CE#=V_{CC}-0.2, WP#=0/V_{CC}	-	10	50	-	10	50		10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vc (max)	-	-	±10	-	-	±10		-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to Vcc(max)	-	-	±10	-	-	±10		-	±10	uA
Input High Voltage		V_{IH}	-	0.8x V_{CC}	-	V_{CC} +0.3	0.8x Vcc	-	V_{CC} +0.3	0.8x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2x V_{CC}	-0.3	-	0.2x V_{CC}	-0.3	-	0.2x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH} = -100uA	V_{CC}-0.1	-	-	V_{CC}-0.4	-	-				V
			I_{OH} = -400uA							2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL} = 100uA	-	-	0.1	-	-	0.4				V
			I_{OL} = 2.1mA							-	-	0.4	V
Output Low Current (RB#)		I_{OL} (RB#)	V_{OL}=0.1V	3	4	-	3	4	-				mA
			V_{OL}=0.4V							8	10	-	mA

Table 16: DC and Operating Characteristics

Parameter	Value		
	1.8Volt	2.7Volt	3.3Volt
Input Pulse Levels	0V to V_{CC}	0V to V_{CC}	0V to V_{CC}
Input Rise and Fall Times	5ns	5ns	5ns
Input and Output Timing Levels	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
Output Load (1.7V – 1.95V & 2.5V - 3.6V)	1 TTL GATE and CL=30pF	1 TTL GATE and CL=30pF	1 TTL GATE and CL=50pF

Table 17: AC Test Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance (1)	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance (1)	C_{IN}	V_{IN} = 0V	-	10	pF

Table 18 : Pin Capacitance (TA = 25C, f=1.0MHz)

NOTE: For the stacked devices version the Input Capacitance is **10pF x <number of stacked chips)** and the I/O capacitance is **10pF x <number of stacked chips)**

Parameter		Symbol	Min	Typ	Max	Unit
Program Time / Multi-plane program Time		t_{PROG}	-	200	700	us
Dummy Busy Time for Two Plane Program		t_{DBSY}	-	0.5	1	us
Cache program short busy time		t_{PCBSY}		3.5	t_{PROG}	us
Number of partial Program Cycles in the same page	Main + Spare Array	NOP	-	-	4	Cycle
Block Erase Time / Multi-plane Erase Time		t_{BERS}	-	2.0	10	ms
Read Cache busy time		t_{RCBSY}		3.5	tR	us
Multi-plane erase short busy time (ONFI protocol only)		t_{IEBSY}		0.5	1	us

Table 19: Program / Erase Characteristics

Parameter	Symbol	1.8 Volt		2.7 Volt		3.3 Volt		Unit
		Min	Max			Min	Max	
CLE Setup time	t_{CLS}	10		10		10		ns
CLE Hold time	t_{CLH}	5		5		5		ns
CE# Setup time	t_{CS}	25		15		15		ns
CE# Hold time	t_{CH}	5		5		5		ns
WE# Pulse width	t_{WP}	15		10		10		ns
ALE Setup time	t_{ALS}	10		10		10		ns
ALE Hold time	t_{ALH}	5		5		5		ns
Data Setup time	t_{DS}	10		7		7		ns
Data Hold time	t_{DH}	5		5		5		ns
Write Cycle time	t_{WC}	30		20		20		ns
WE# High Hold time	t_{WH}	10		7		7		ns
Address to Data Loading time	t_{ADL}	100		70		70		ns
Data Transfer from Cell to Register	t_R		25		25		25	us
ALE to RE# Delay	t_{AR}	10		10		10		ns
CLE to RE# Delay	t_{CLR}	10		10		10		ns
Ready to RE# Low	t_{RR}	20		20		20		ns
RE# Pulse Width	t_{RP}	15		10		10		ns
WE# High to Busy	t_{WB}		100		100		100	ns
Read Cycle Time	t_{RC}	30		20		20		ns
RE# Access Time	t_{REA}		30		20		20	ns
CE# Access Time	t_{CEA}		45		25		25	ns
RE# High to Output Hi-Z	t_{RHZ}		100		100		100	ns
CE# High to Output Hi-Z	t_{CHZ}		30		30		30	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10		10		10		ns
RE# High to Output Hold	t_{RHOH}	15		15		15		ns
RE# Low to Output Hold	t_{RLOH}	-		5		5		ns
CE# High to Output Hold	t_{COH}	15		15		15		ns
RE# High Hold Time	t_{REH}	10		7		7		ns
Output Hi-Z to RE# Low	t_{IR}	0		0		0		ns
RE# High to WE# Low	t_{RHW}	100		100		100		ns
WE# High to RE# Low	t_{WHR}	60		60		60		ns
Device Resetting Time (Read/Program/Erase)	t_{RST}		5/10/500 (1)		5/10/500 (1)		5/10/500 (1)	us
Write protection time	t_{WW}	100		100		100		ns

Table 20 : AC Timing Characteristics

NOTE:
(1) If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us

5 Timing Diagrams

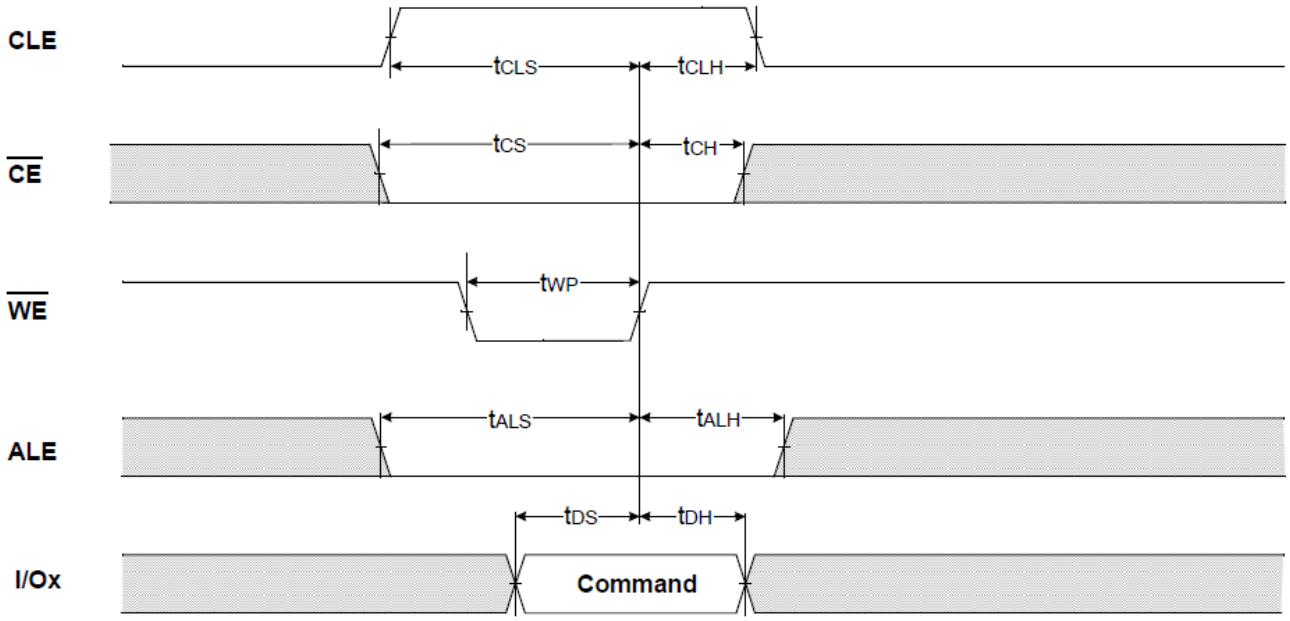


Figure 3 : Command Latch Cycle

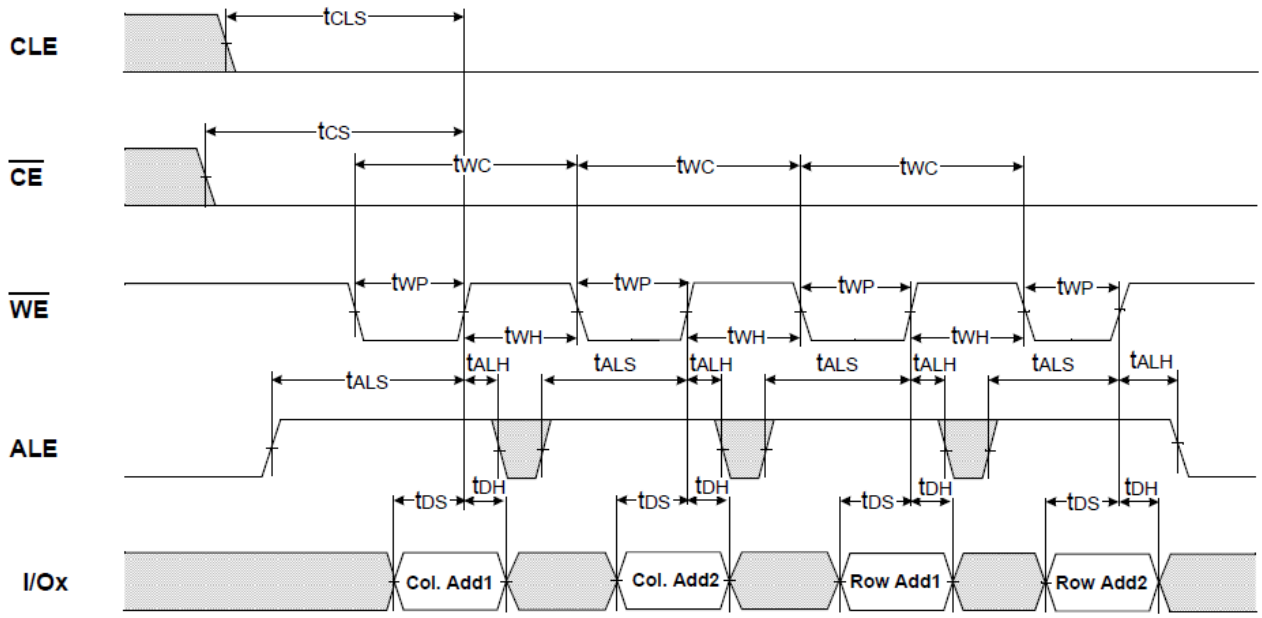


Figure 4 : Address Latch Cycle

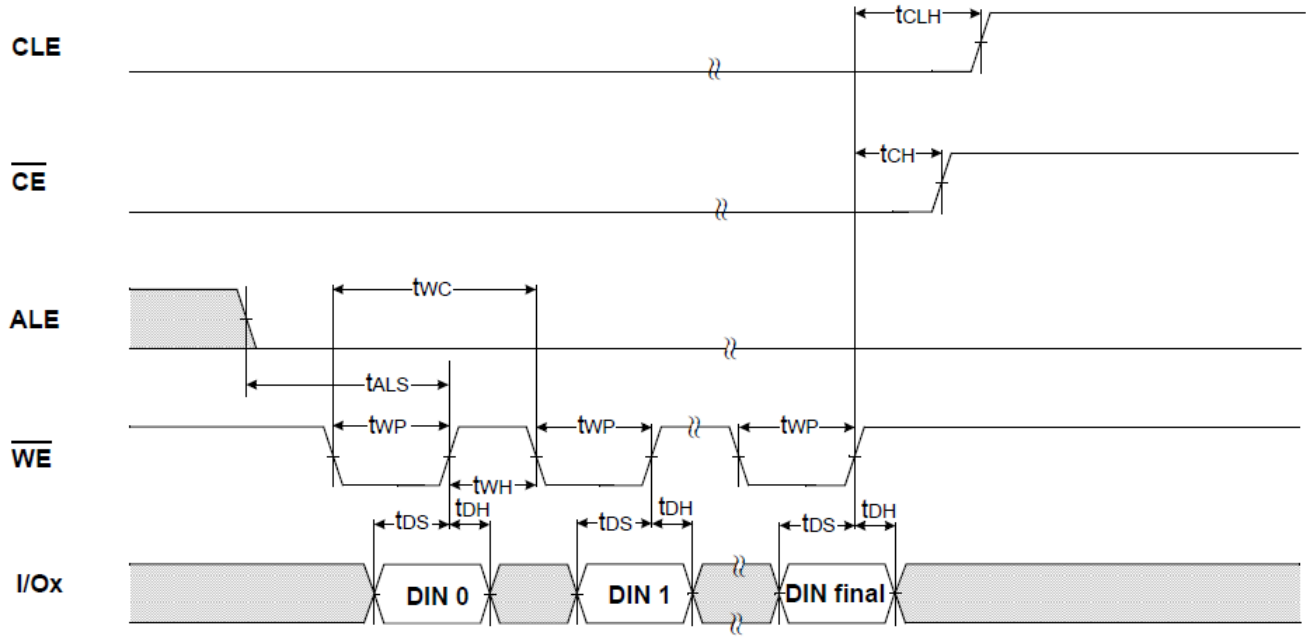
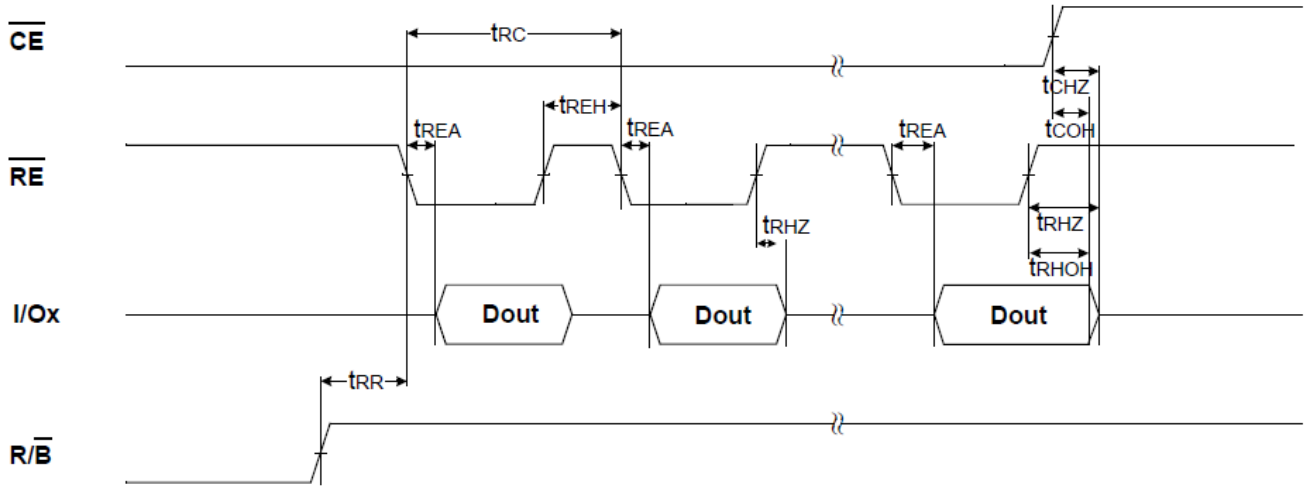
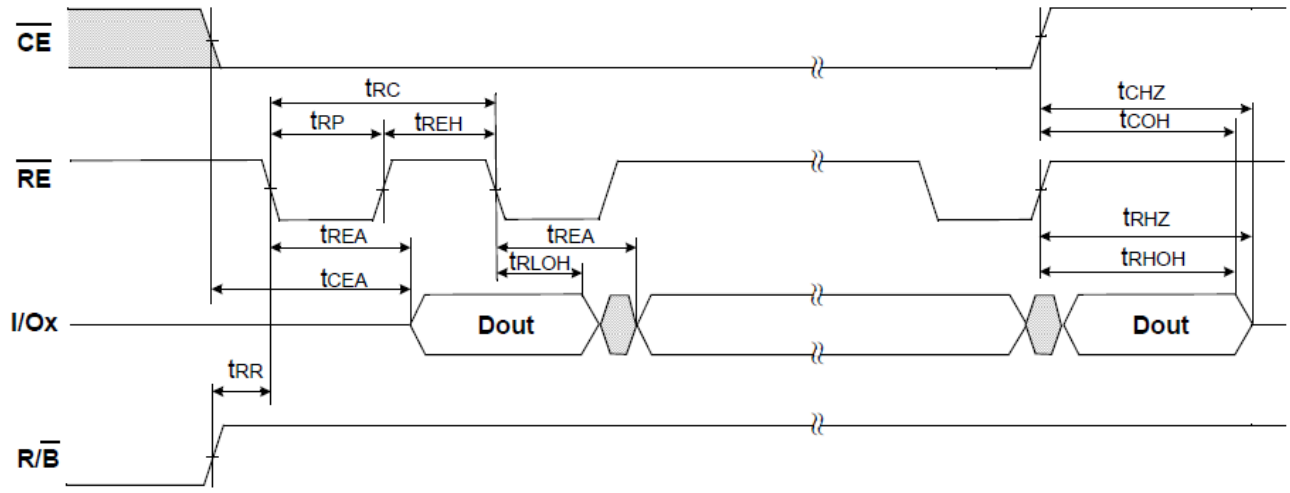


Figure 5 : Input Data Latch Cycle



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 6 : Sequential Out Cycle after Read



NOTES : Transition is measured at ±200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 7 : Sequential Out Cycle after Read

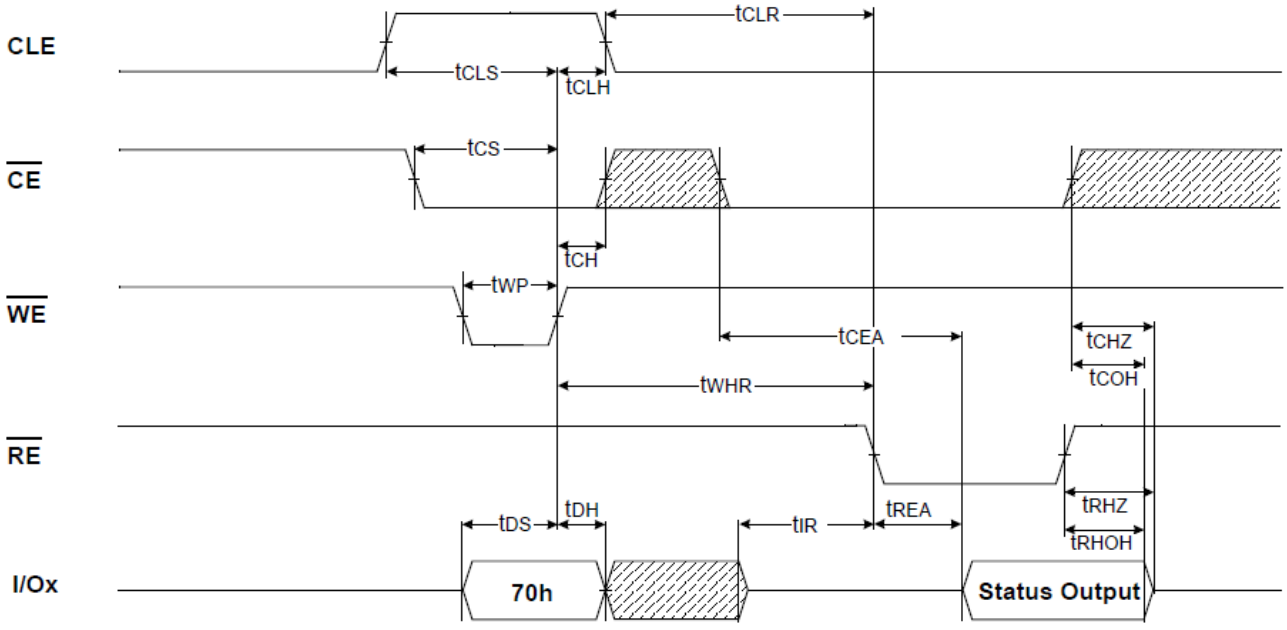


Figure 8 : Status Read Cycle

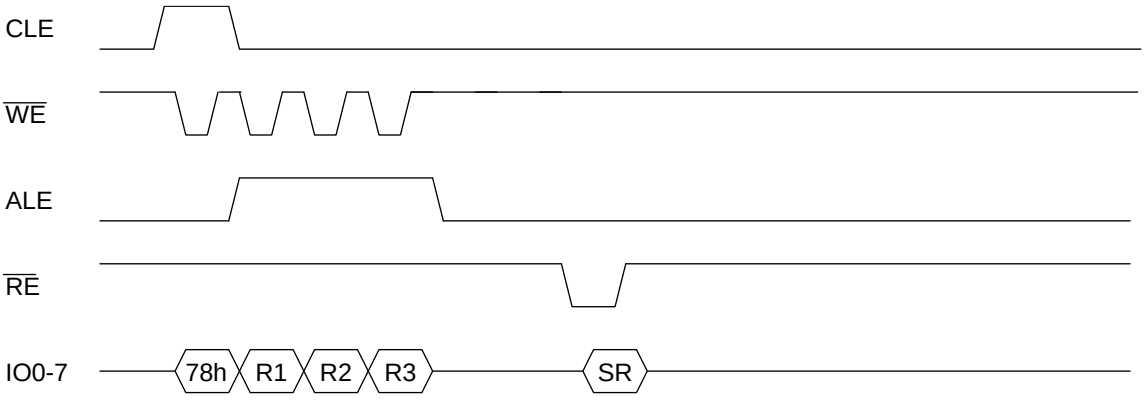


Figure 9: Read Status Enhanced cycle

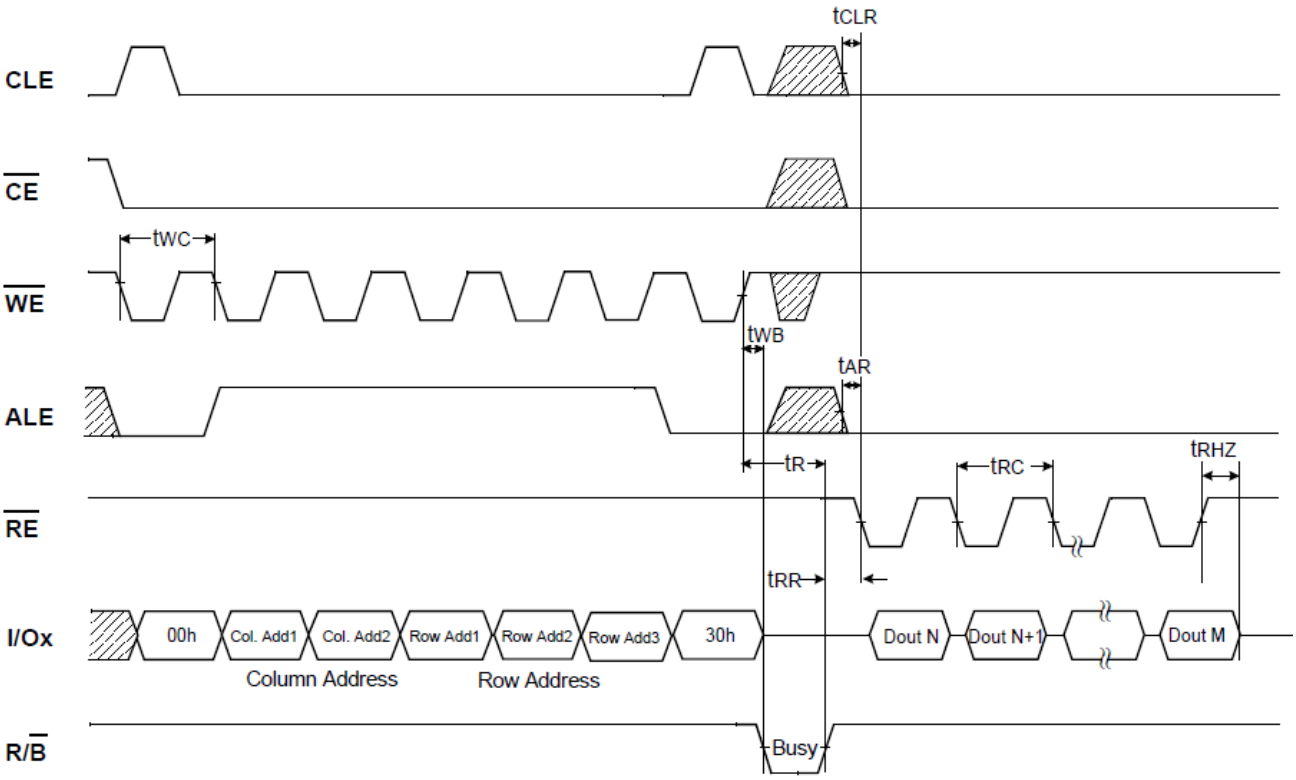


Figure 10 : Read Operation (Read One Page)

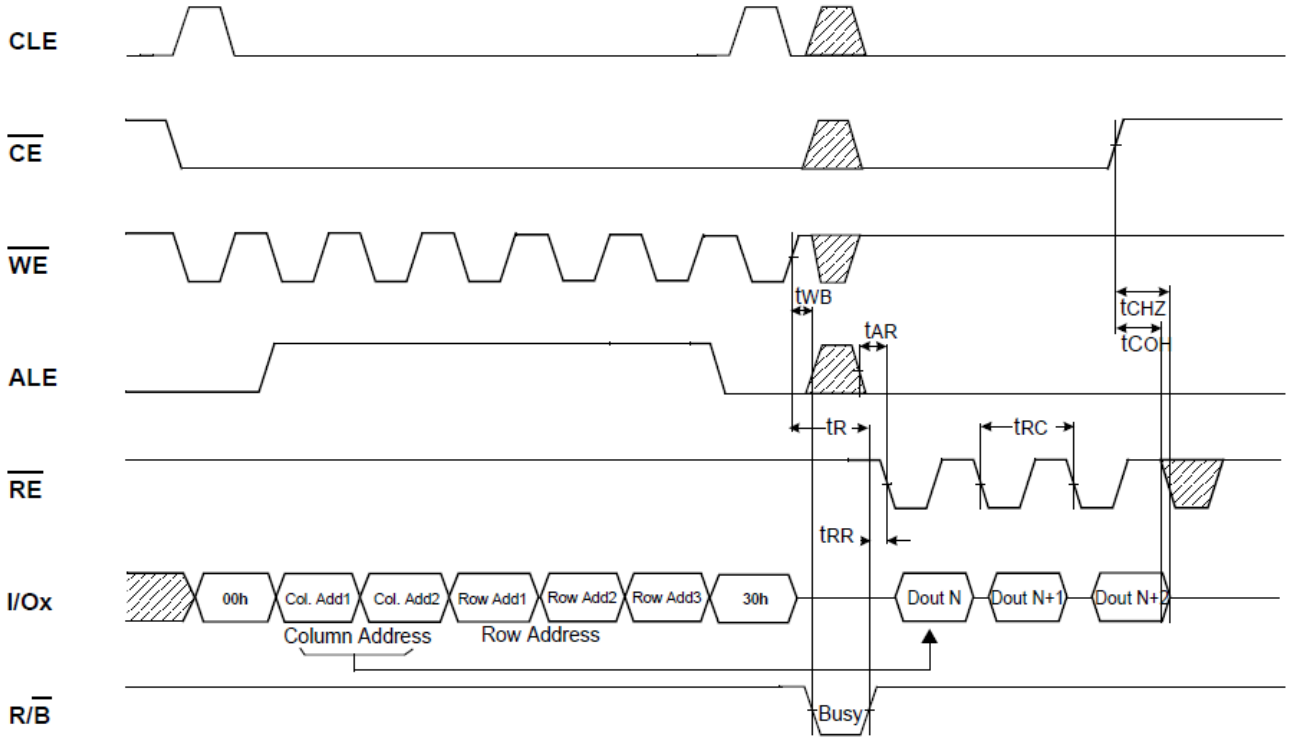


Figure 11 : Read Operation intercepted by CE#

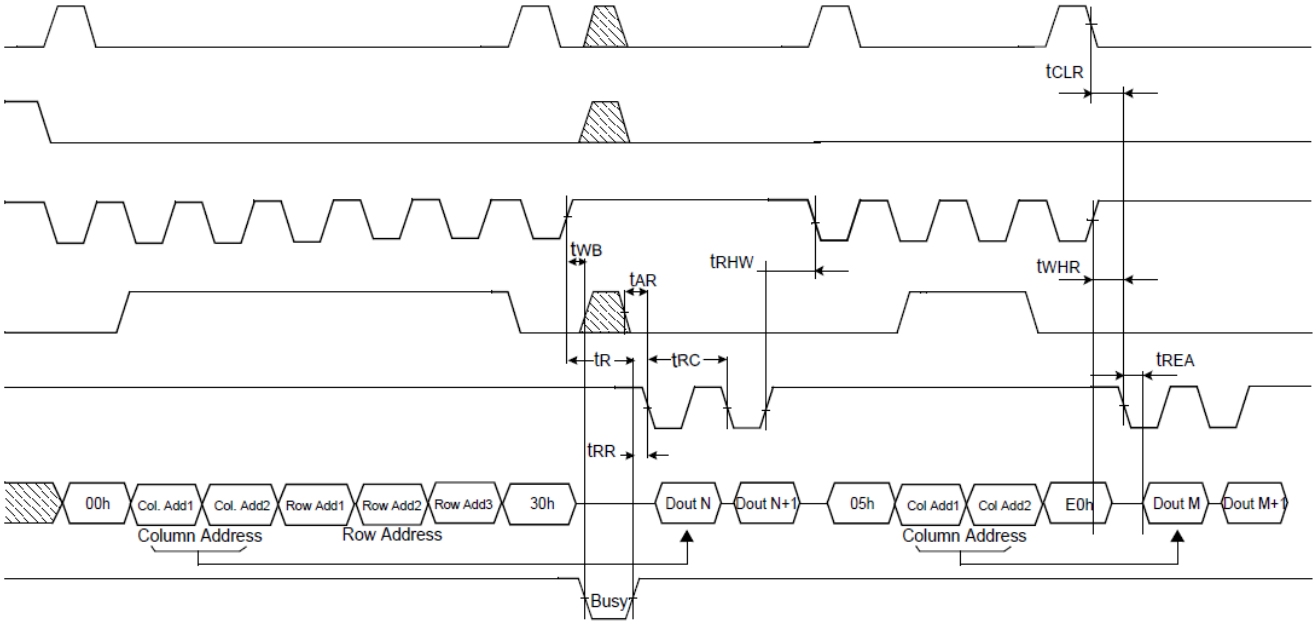


Figure 12 : Random Data Output

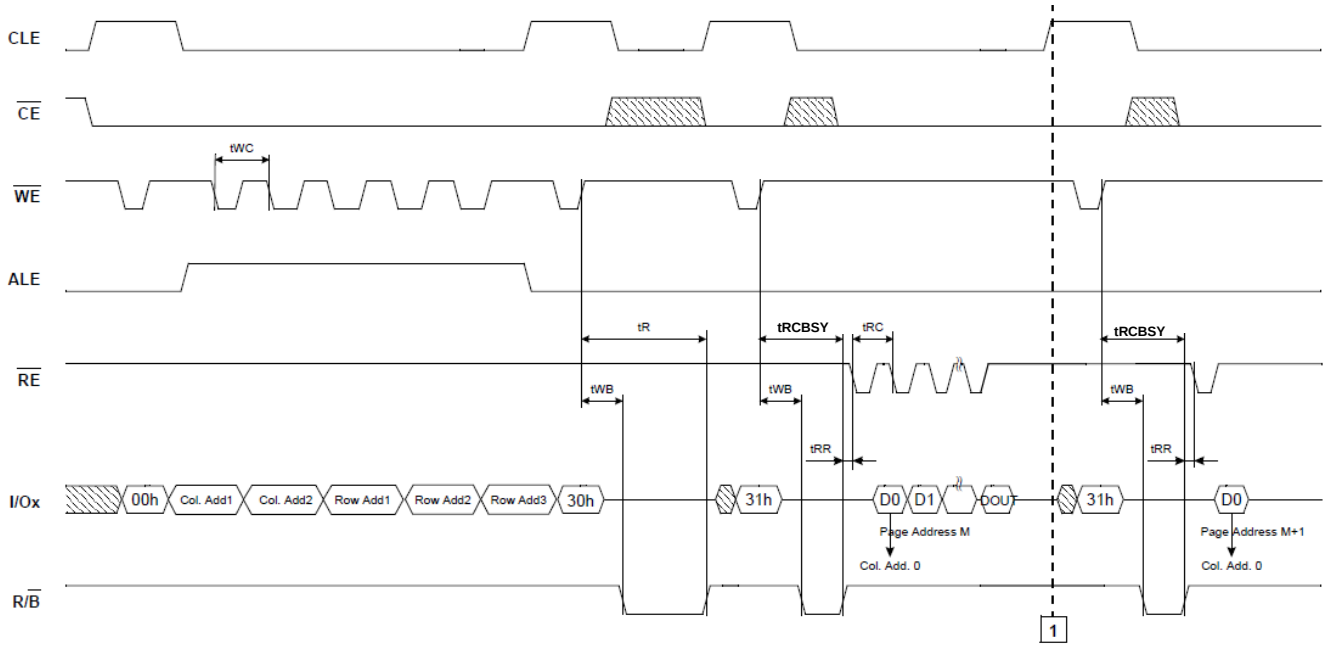


Figure 13 : read cache timings, start of cache operation

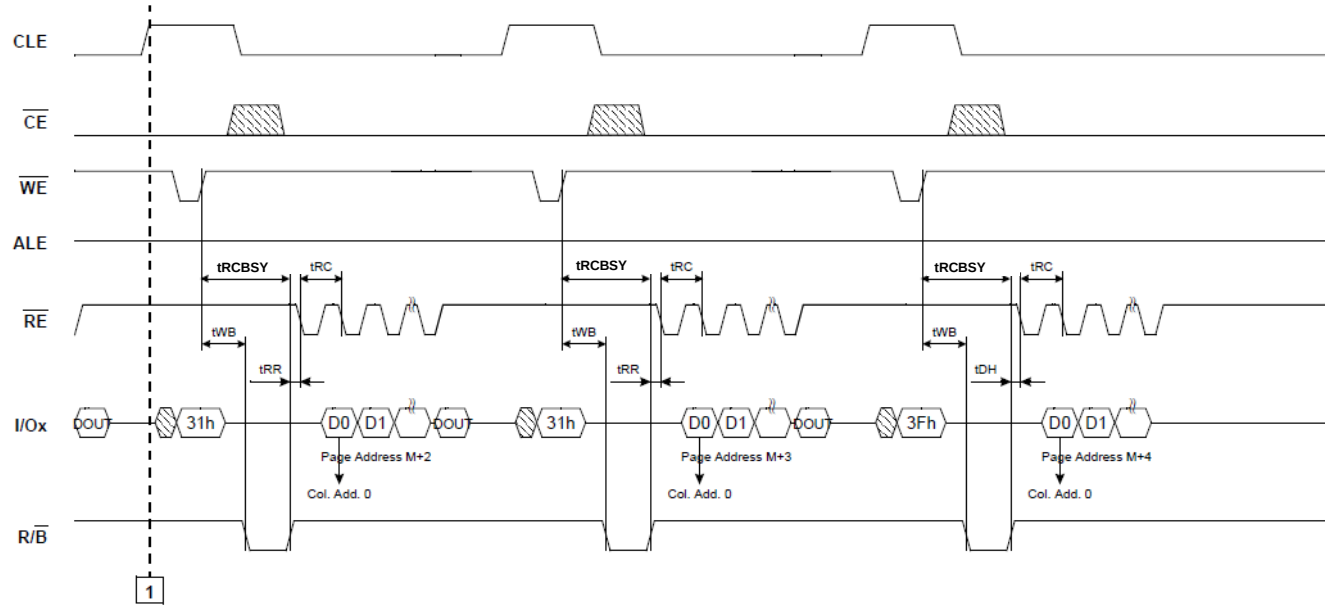


Figure 14 : read cache timings, end of cache operation

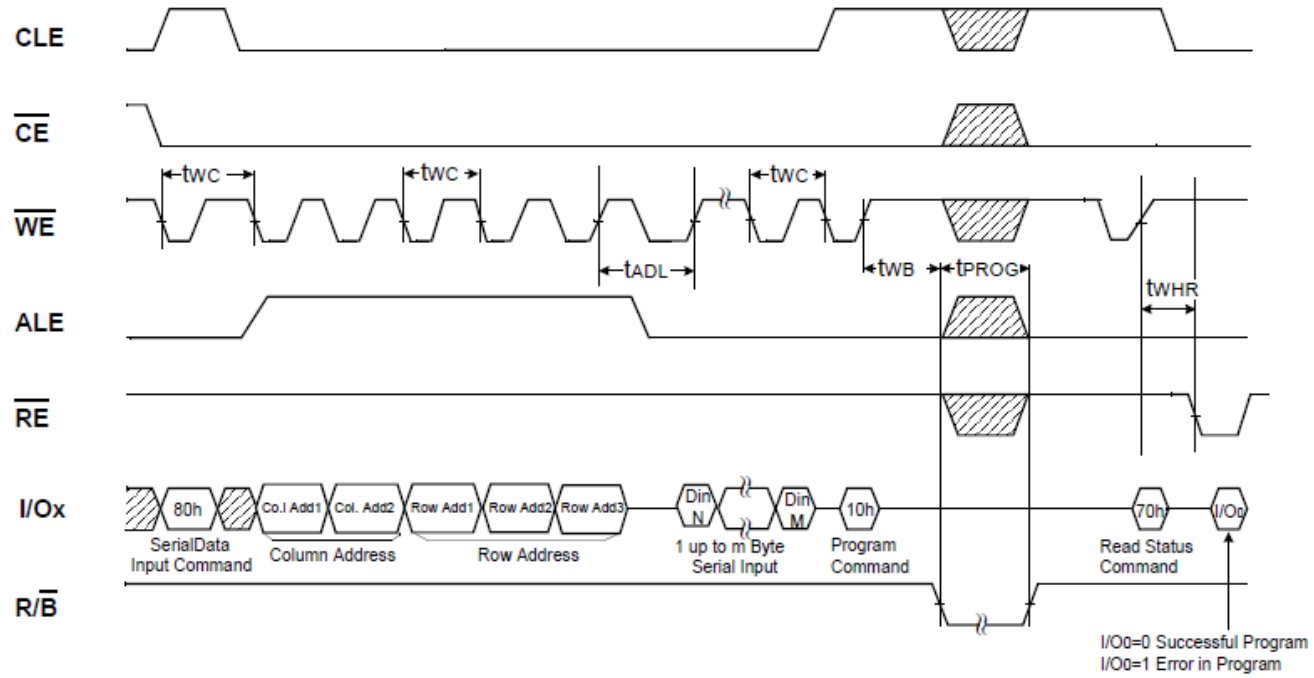


Figure 15 : Page Program Operation

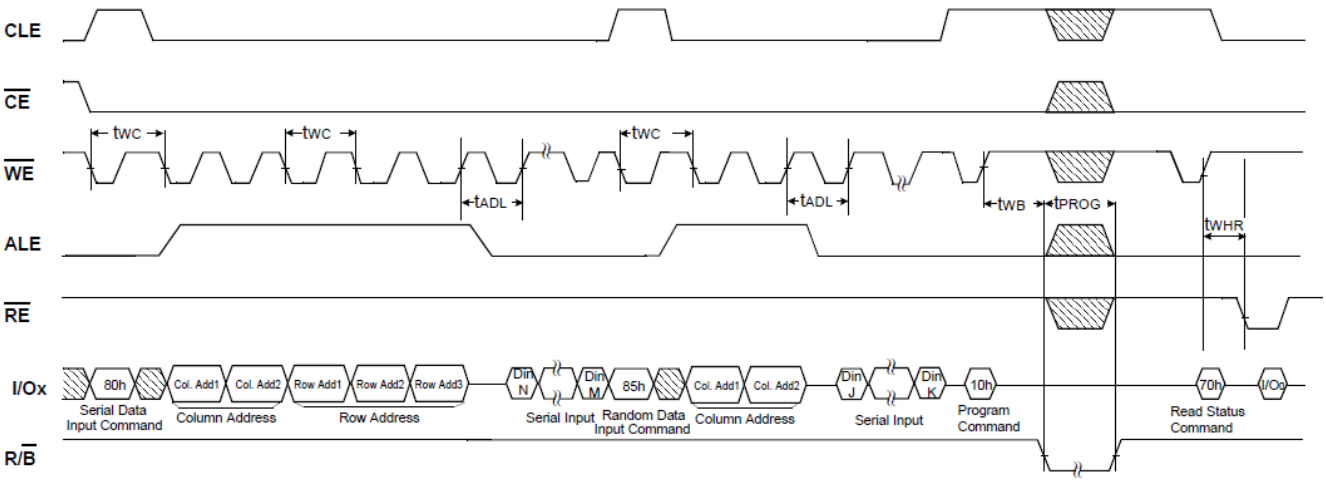


Figure 16 : Random Data In

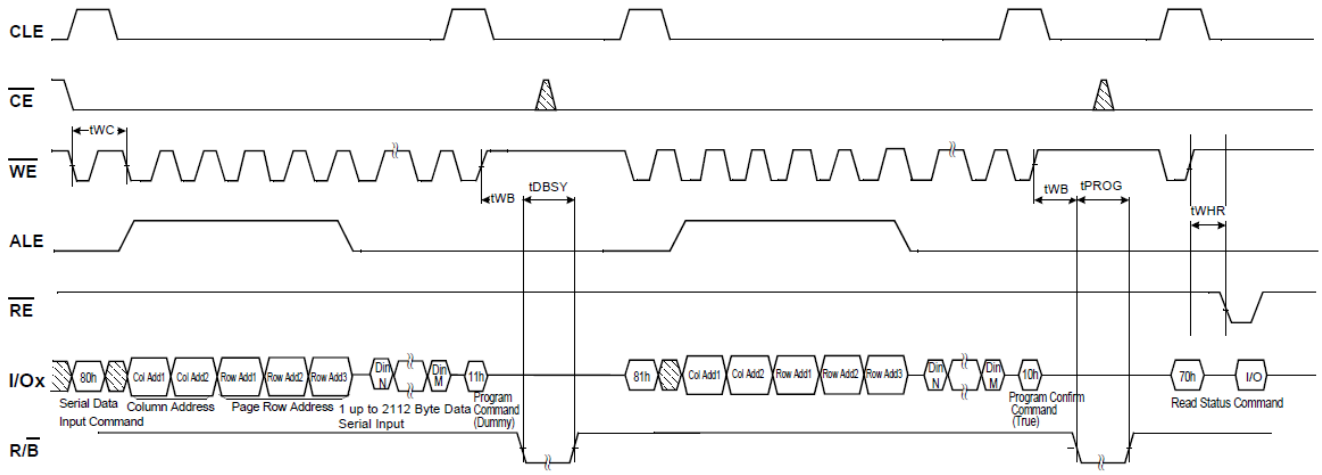


Figure 17 : multi-plane program

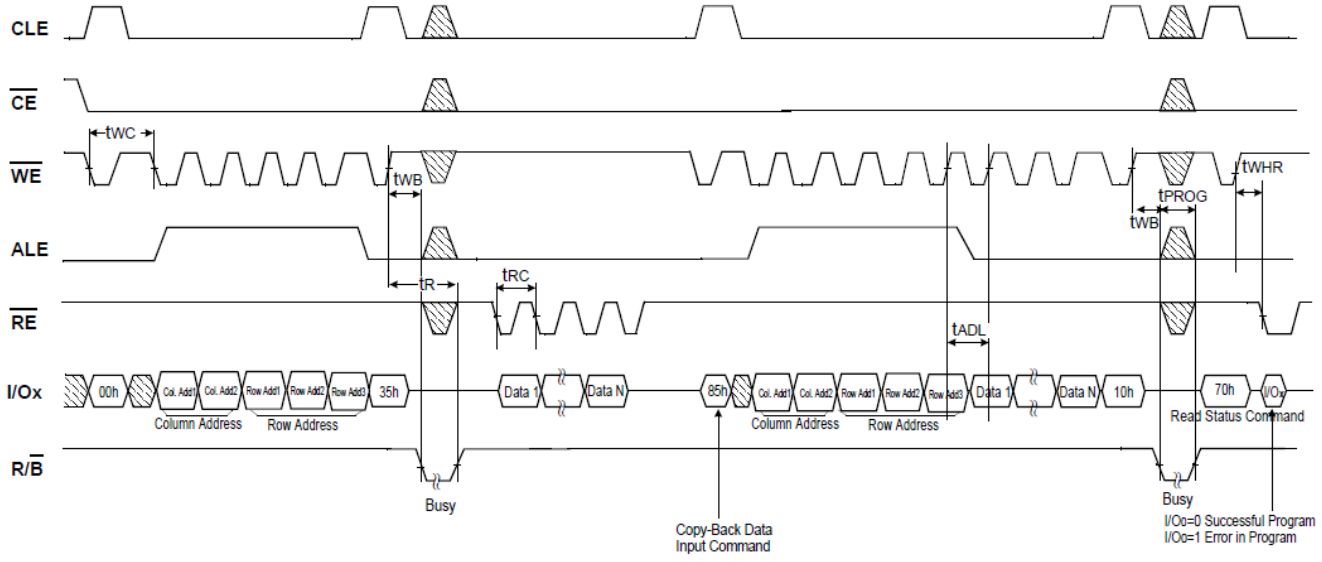


Figure 18 : Copy Back read with optional data readout /Copy back program with optional data input

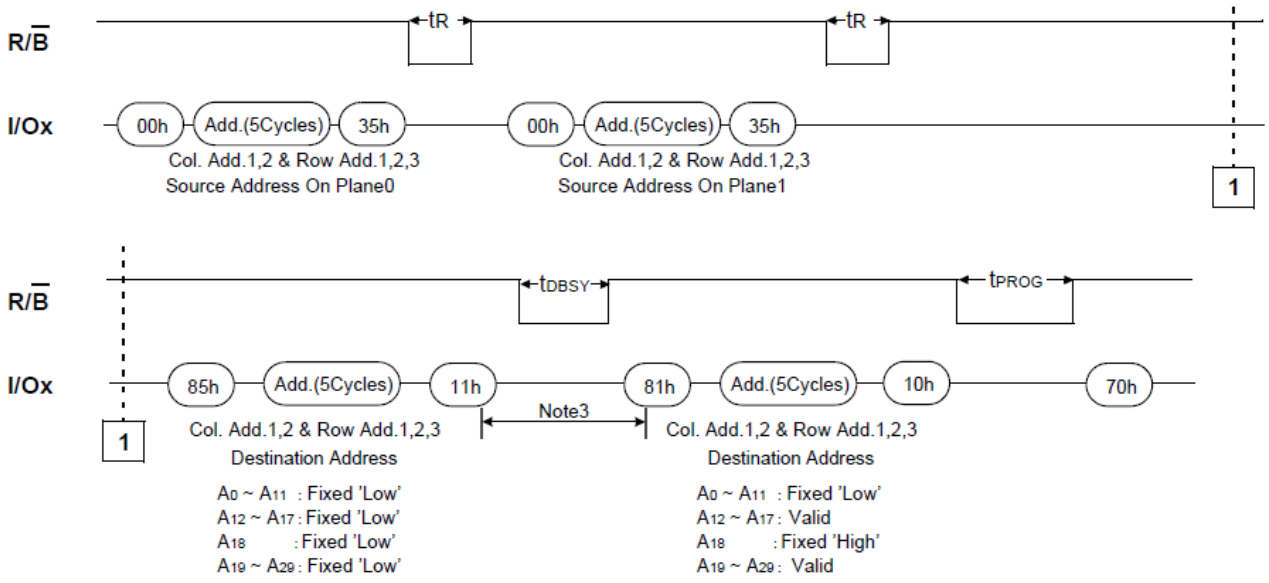


Figure 19 : multi-plane copyback program

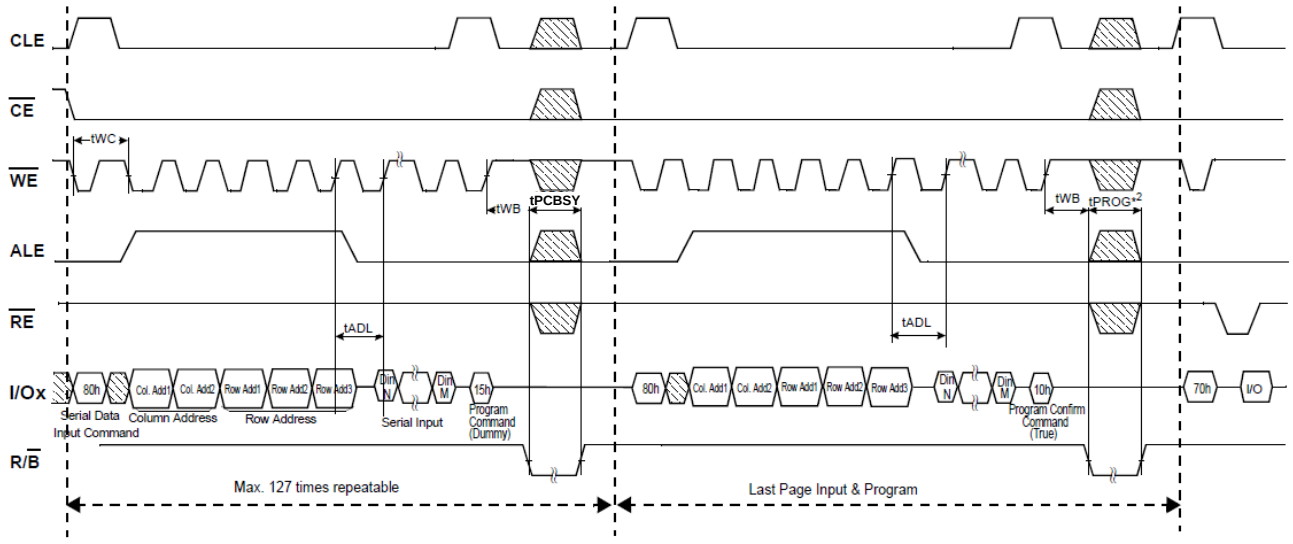


Figure 20 : cache program

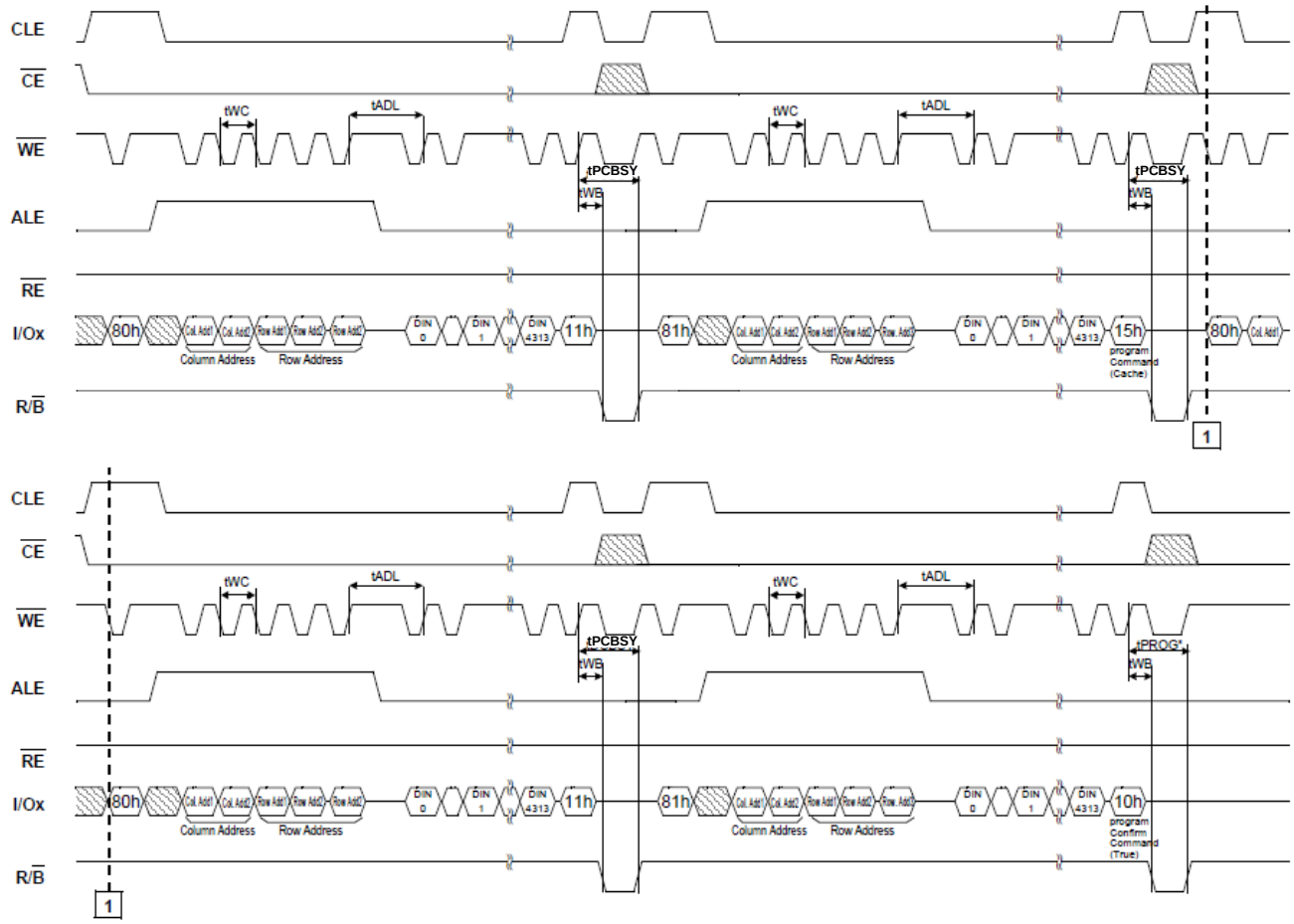


Figure 21 : multi-plane cache program

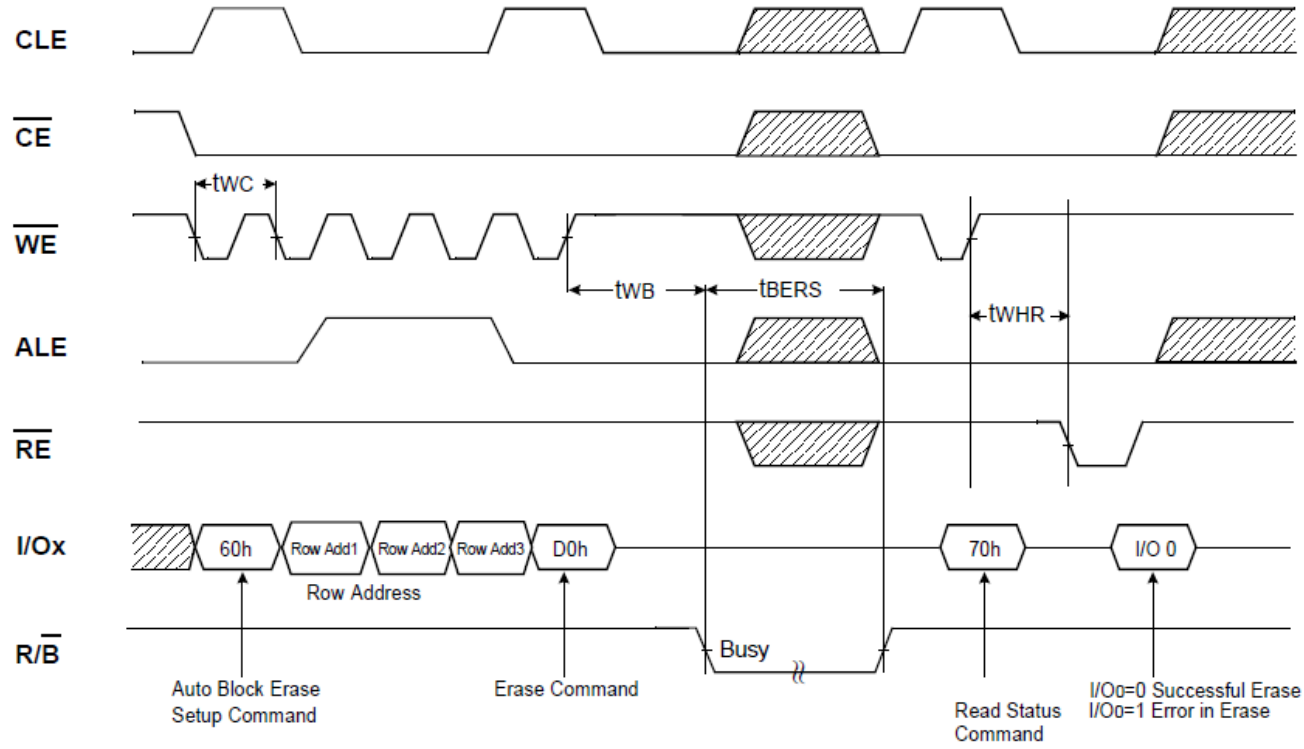


Figure 22 : Block Erase Operation (Erase One Block)

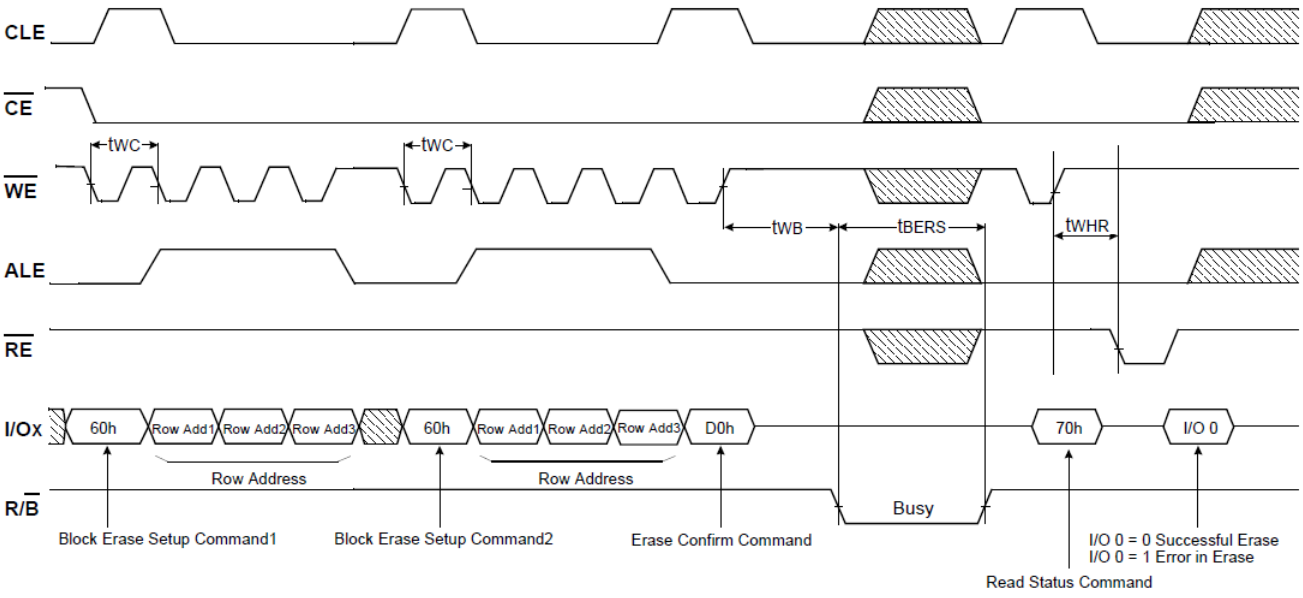


Figure 23 : multi-plane block erase

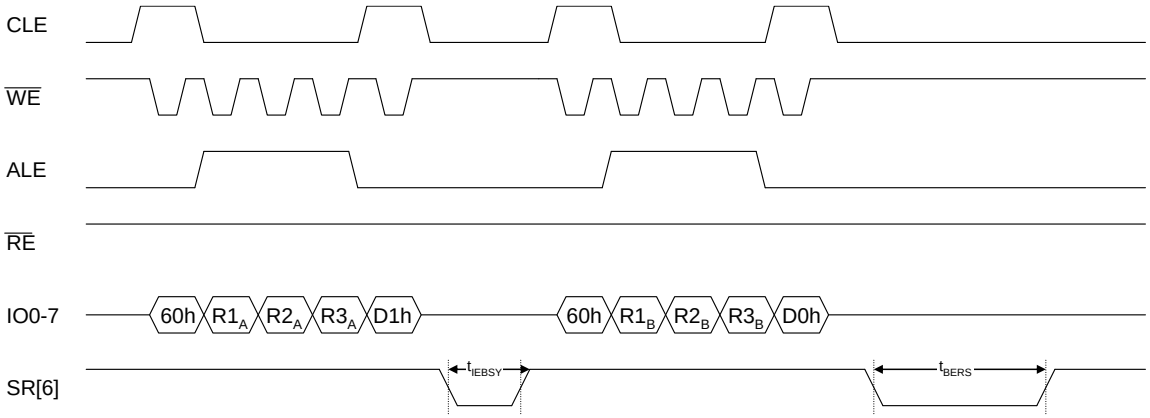


Figure 24: Multiple plane block erase (ONFI 1.0 protocol)

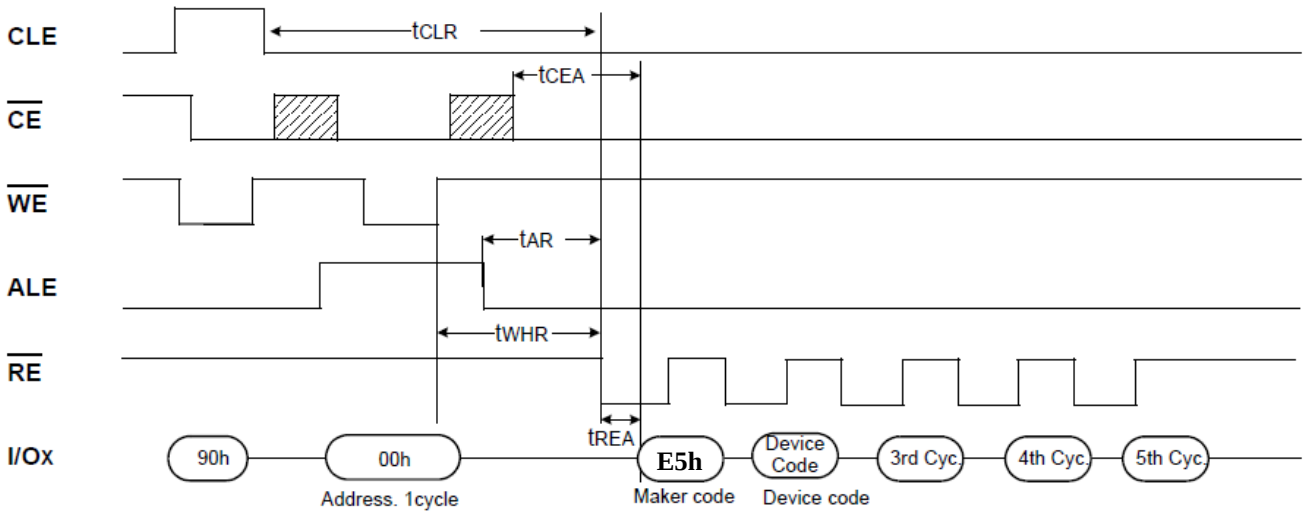


Figure 25 : READ ID Operation

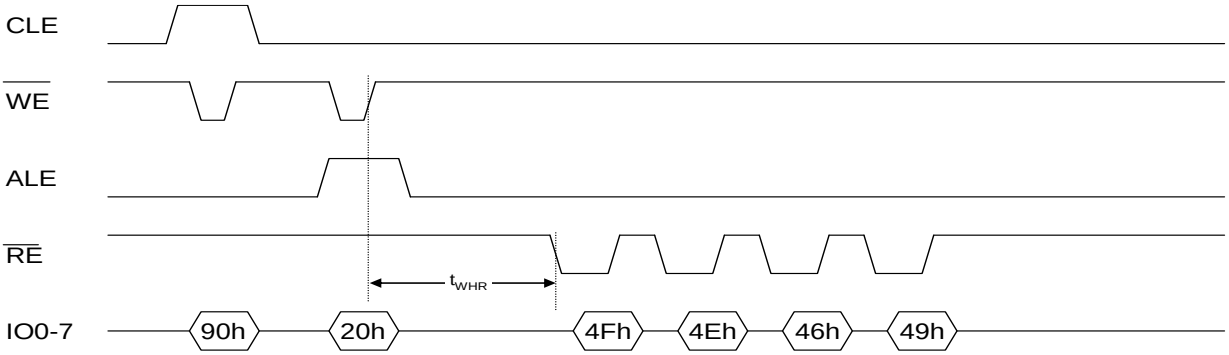


Figure 26 : ONFI signature timing diagram

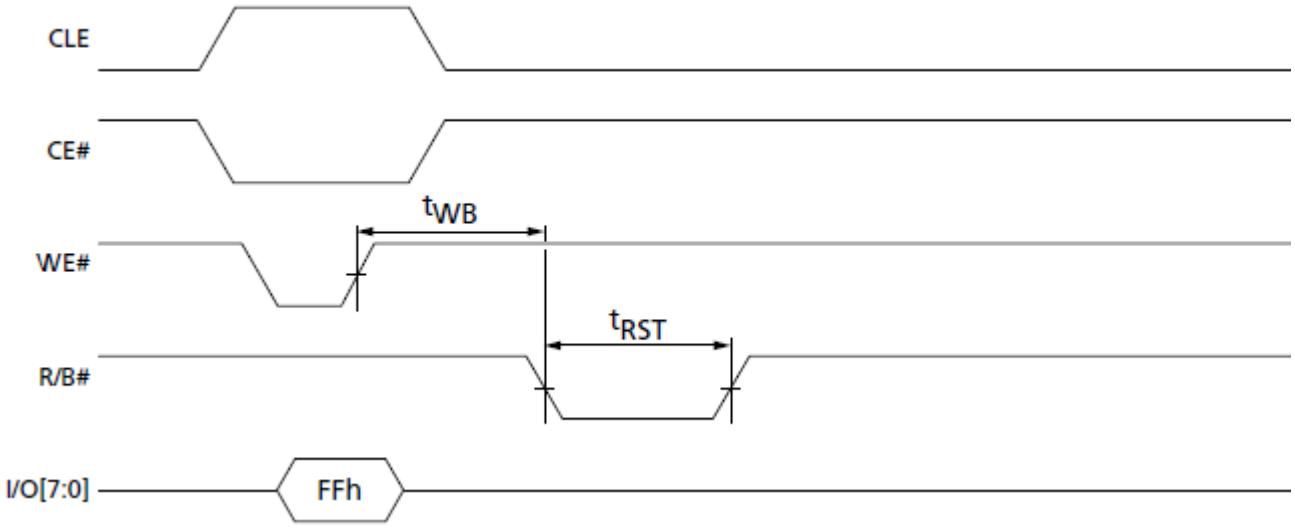


Figure 27 : Reset operation timing

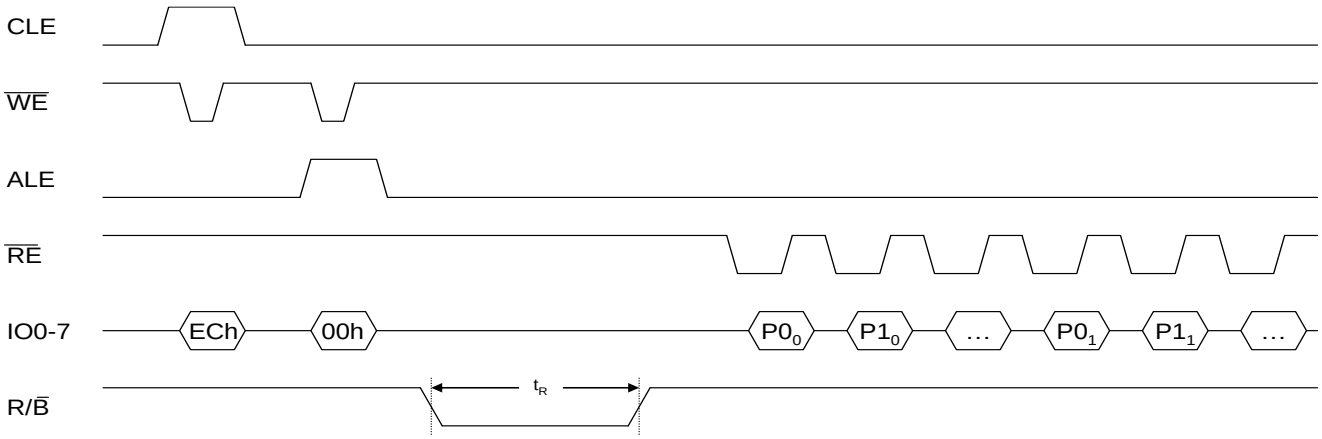


Figure 28 : Read Parameter Page timings

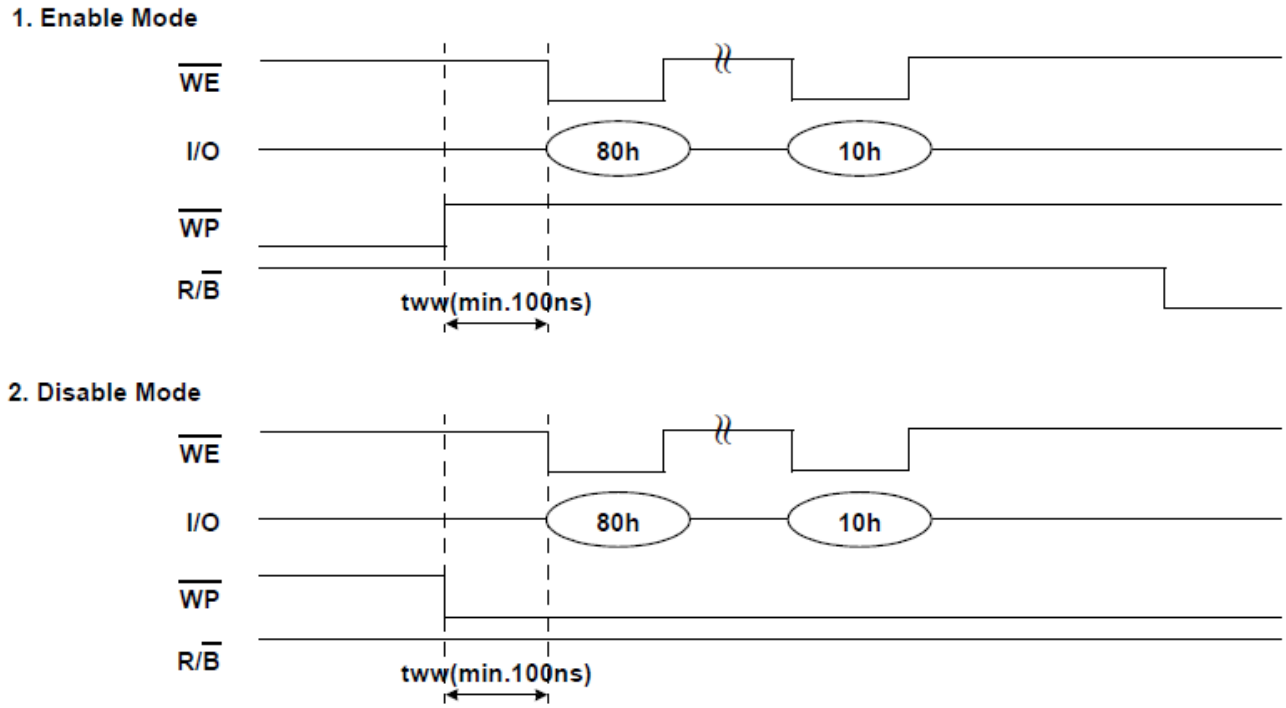


Figure 29 : tWW in Program Operation

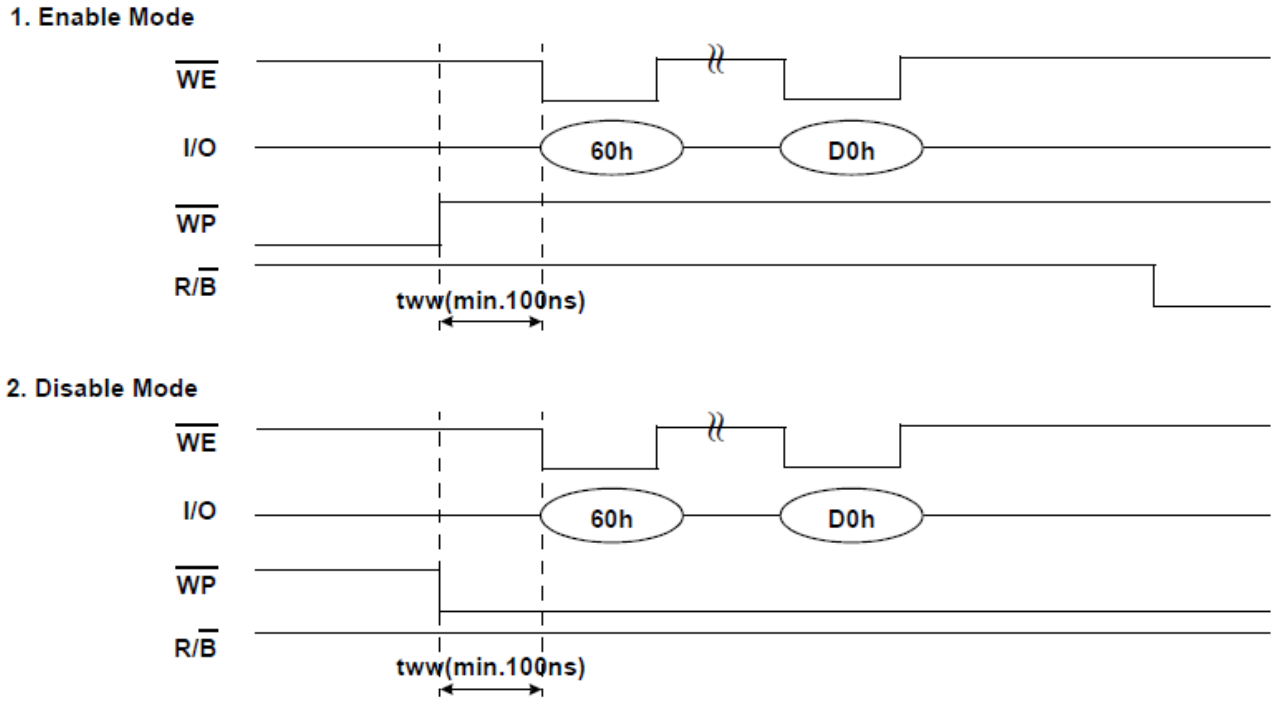


Figure 30 : tWW in Erase Operation

Note : V_{TH} = 1.5 Volt for 1.8 Volt Supply devices; 2.5 Volt for 3.3 Volt Supply devices

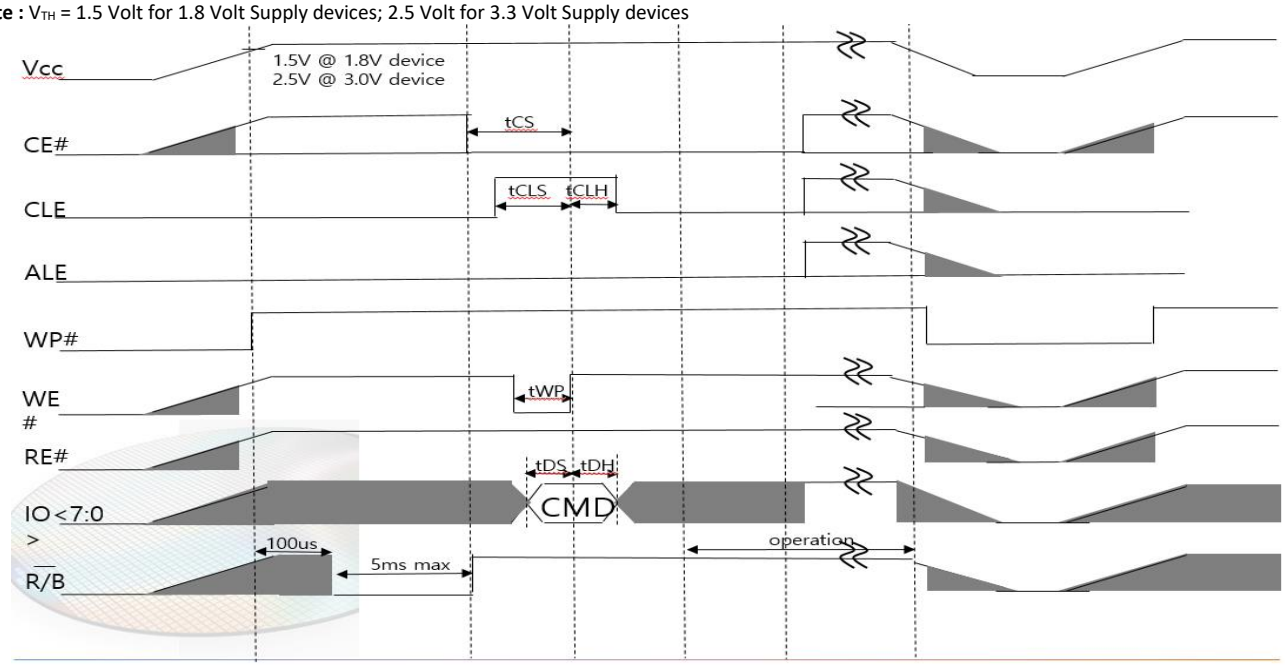
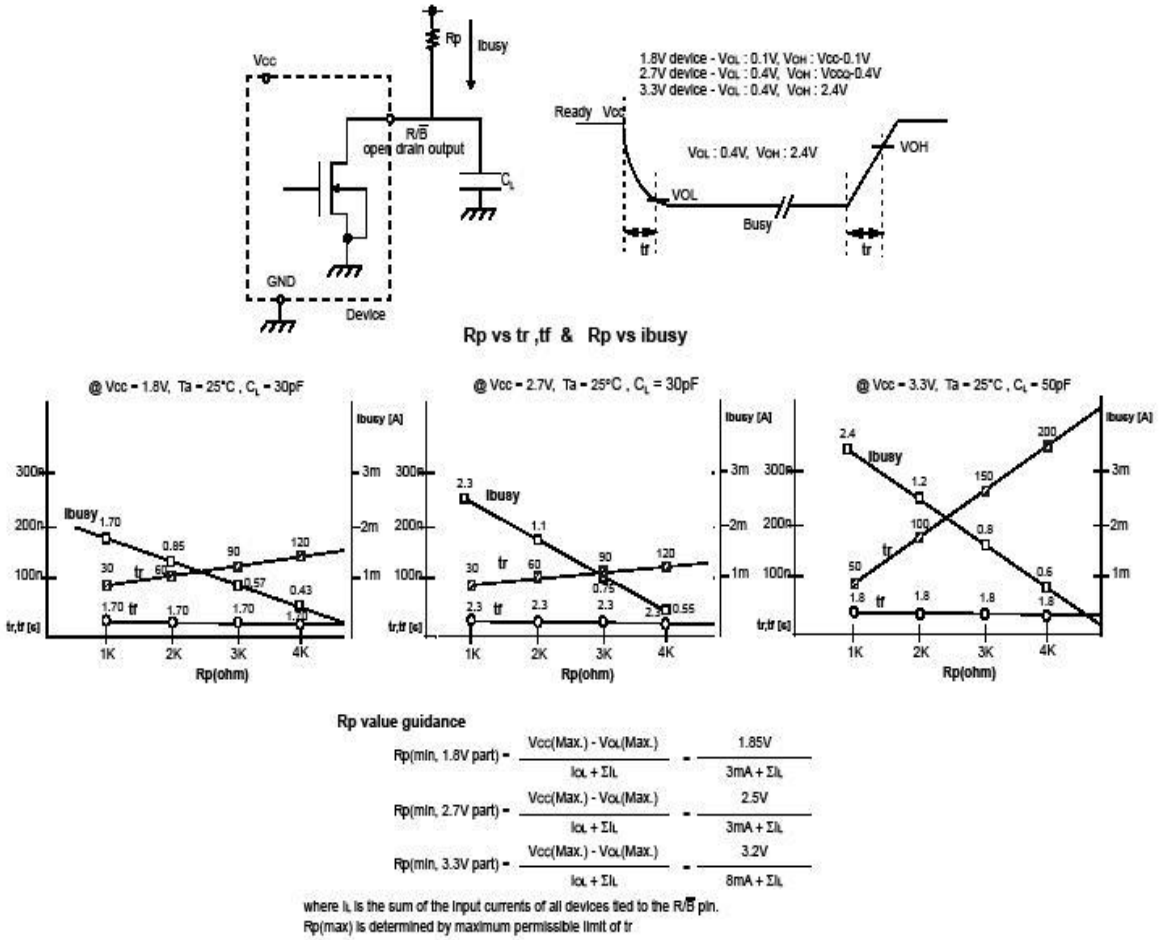


Figure 31 : Power up time sequence



Rp value guidance

$$Rp(min,\ 1.8V\ part) = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3mA + \Sigma I_L}$$

$$Rp(min,\ 2.7V\ part) = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{2.5V}{3mA + \Sigma I_L}$$

$$Rp(min,\ 3.3V\ part) = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/$\overline{B}$ pin.
Rp(max) is determined by maximum permissible limit of tr

Figure 32 : Ready/Busy Pin electrical application

6 Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the 1st or 2nd page (if the 1st page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart

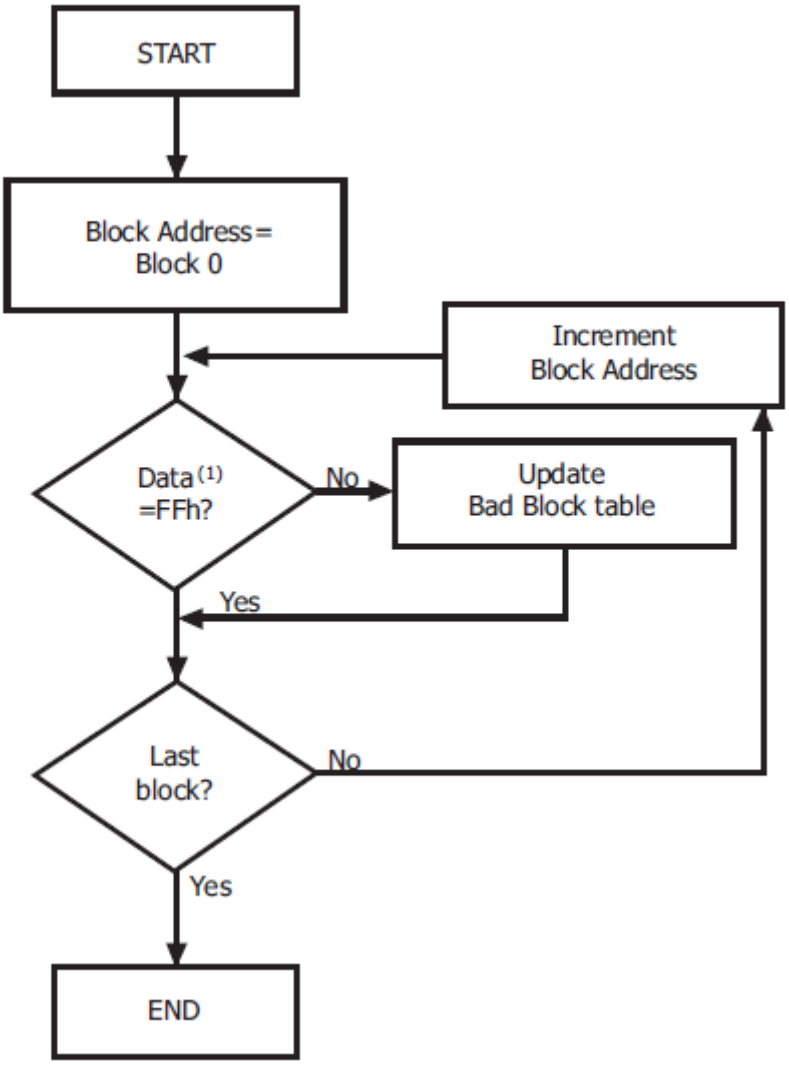


Figure 33 : Bad Block Management Flowchart

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
The failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Failure Mode		Detection and Countermeasure sequence
Write	Erase Failure	Status Read after Erase --> Block Replacement
	Program Failure	Status Read after Program --> Block Replacement
Read	Single Bit Failure	Verify ECC -> ECC Correction

Figure 34 : Block Failure

Block Replacement flow is as below
1.When an error happens in the nth page of the Block 'A' during erase or program operation.
2.Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
3.Copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
4.Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

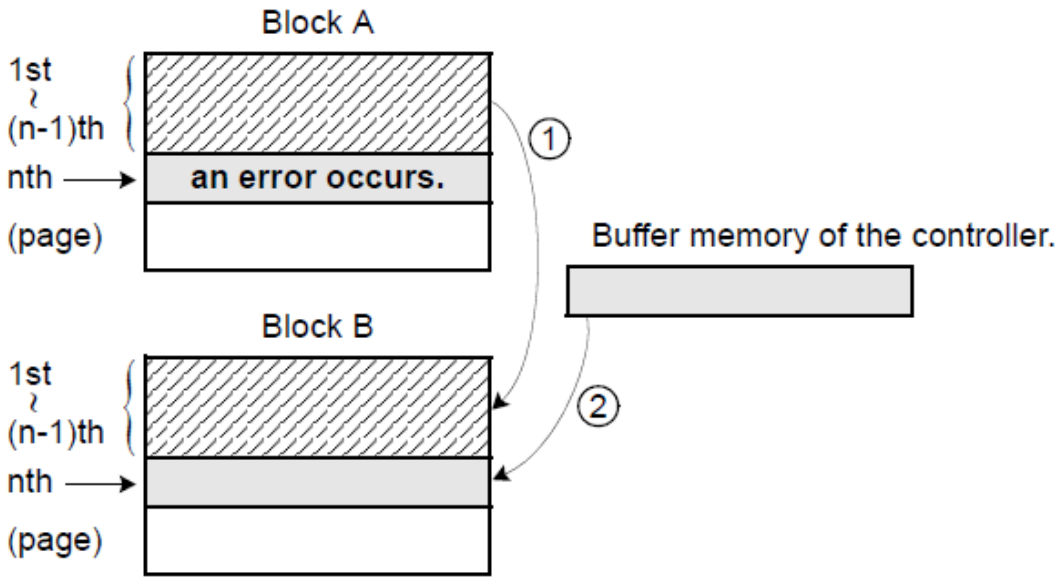
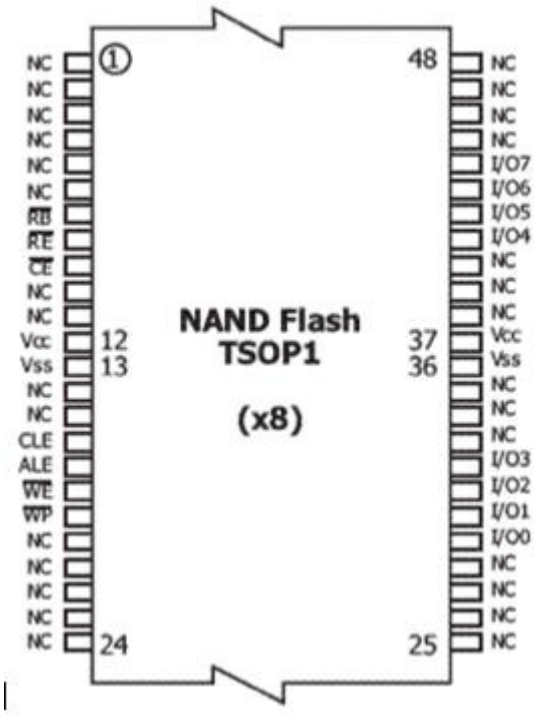


Figure 35 : Bad Block Replacement

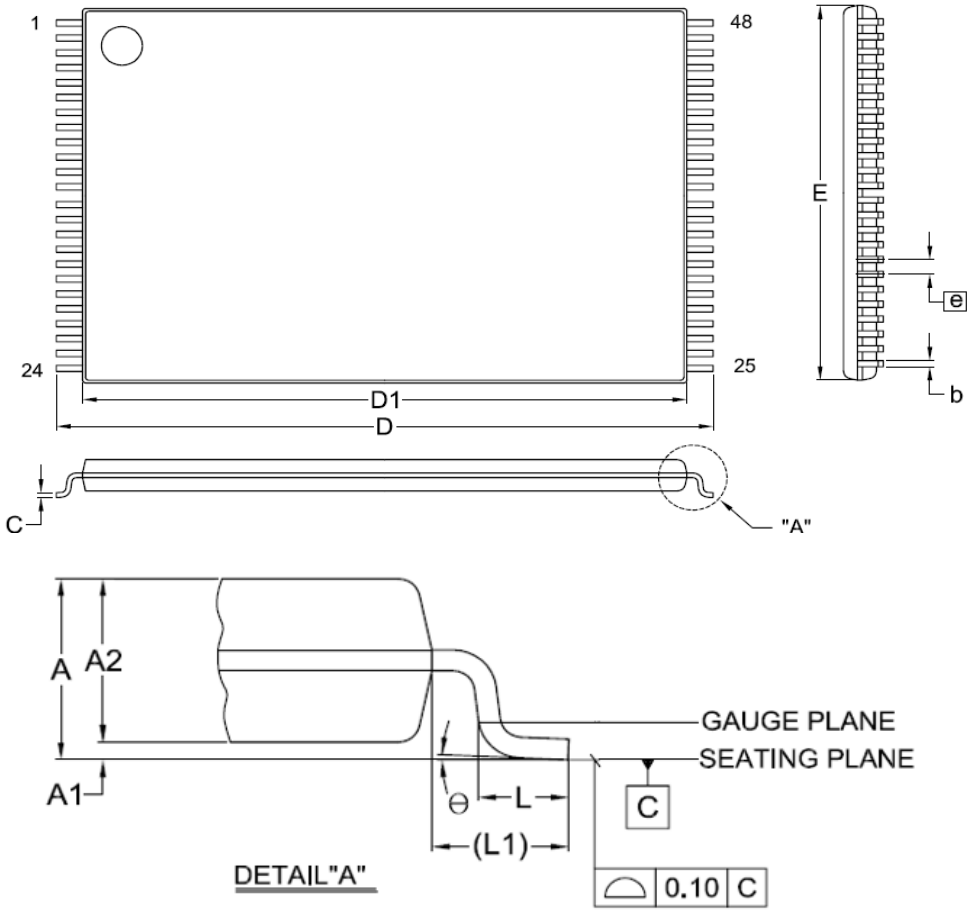
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7 Supported Packages

7.1 PIN CONFIGURATION (TSOP1)



PACKAGE DIMENSIONS
48-PIN LEAD/LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

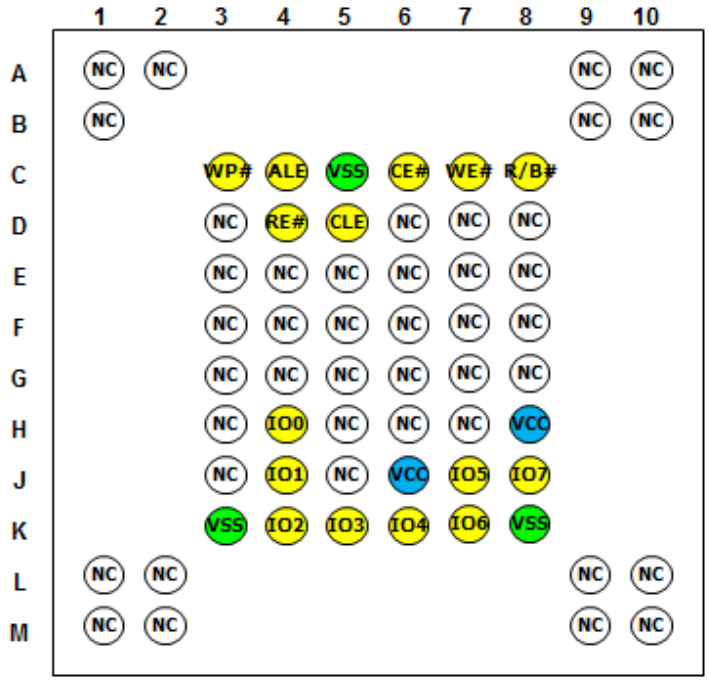


Symbol	Dimension(mm)		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	-	0.27
c	0.10	-	0.21
D	19.90	20.00	20.10
D1	18.30	18.40	18.50
E	11.90	12.00	12.10
e	0.50 BSC		
L	0.50	0.60	0.70
L1	0.80 REF		
θ	0°	-	8°

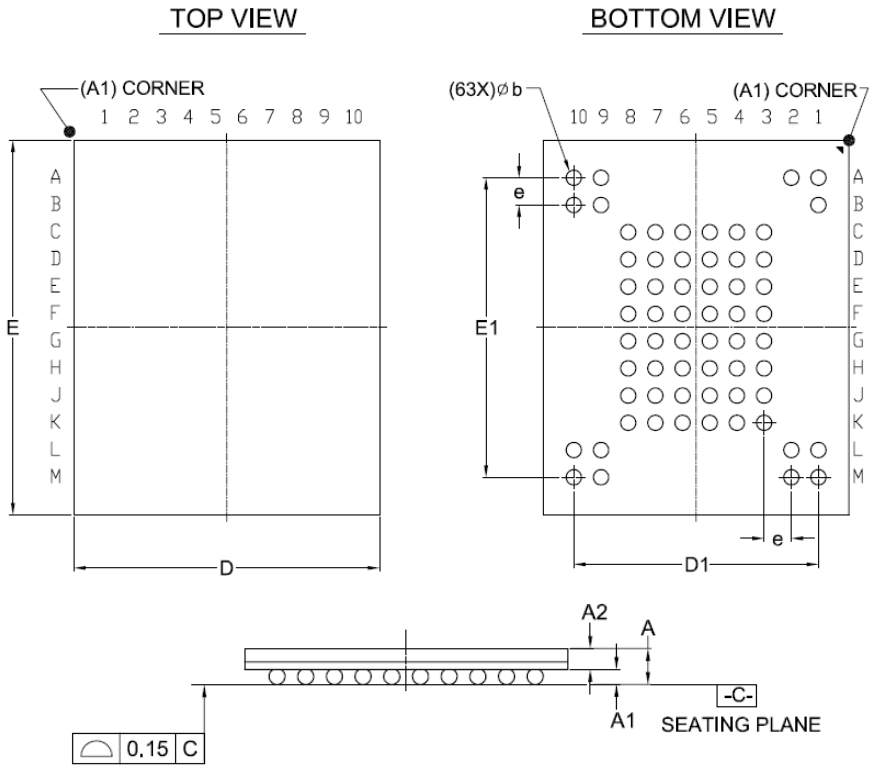
The shape may be of little difference according to different package lead frames/substrates. These shapes are compatible with each other.

7.2 Ball Assignment: 63-Ball FBGA (Balls Down, Top View)

x8



PACKAGE DIMENSIONS
63-Ball FBGA PACKAGE TYPE



Symbol	Dimension(mm)		
	MIN	NOM	MAX
A	-	-	1.00
A1	0.25	0.30	0.40
A2	0.53	-	-
b	0.35	-	0.50
D	8.90	9.00	9.10
D1	7.20 BSC		
E	10.90	11.00	11.10
E1	8.80 BSC		
e	0.80 BSC		

The shape may be of little difference according to different package lead frames/substrates. These shapes are compatible with each other.